



LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : BOT

### Power Source

O2Micro OZ8681

System Charge Power (+BATCHG)

P2806

**System Discharge Power  
(+1.5V/+3V/+5V)**

Ricktek RT8205

System Power (+3VPCU/+5VPCU/  
+3VS5/+5VS5)

**NCP6132/NCP5911/RT8209/G9334**

Processor Power (+VCC\_CORE/  
+1.05\_VTT/+VCCSA)

Richtek RT8207

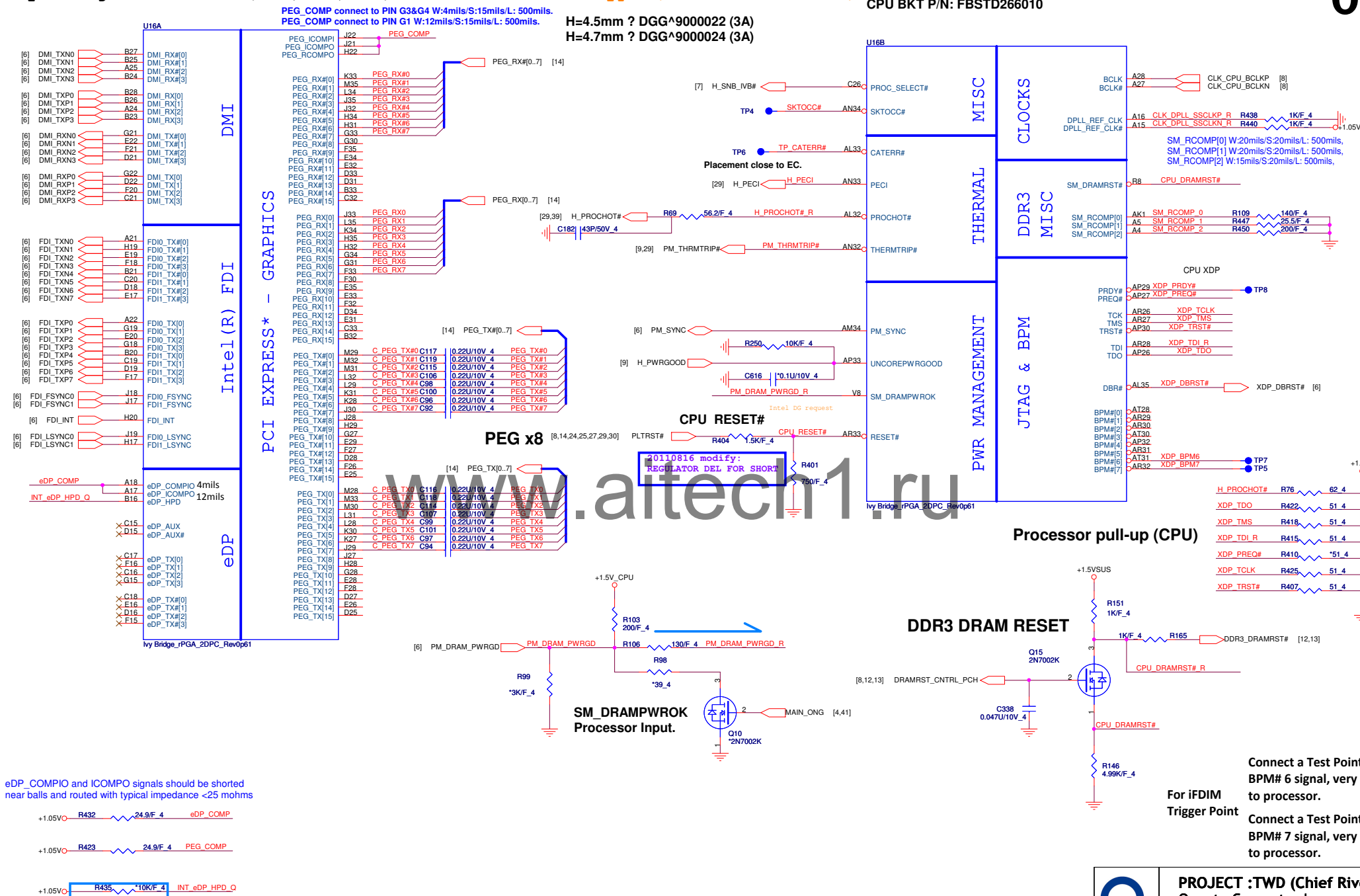
System Memory Power (+1.5VSUS/  
+0.75V\_DDR\_VTT)

Richtek RT8209/RT9025

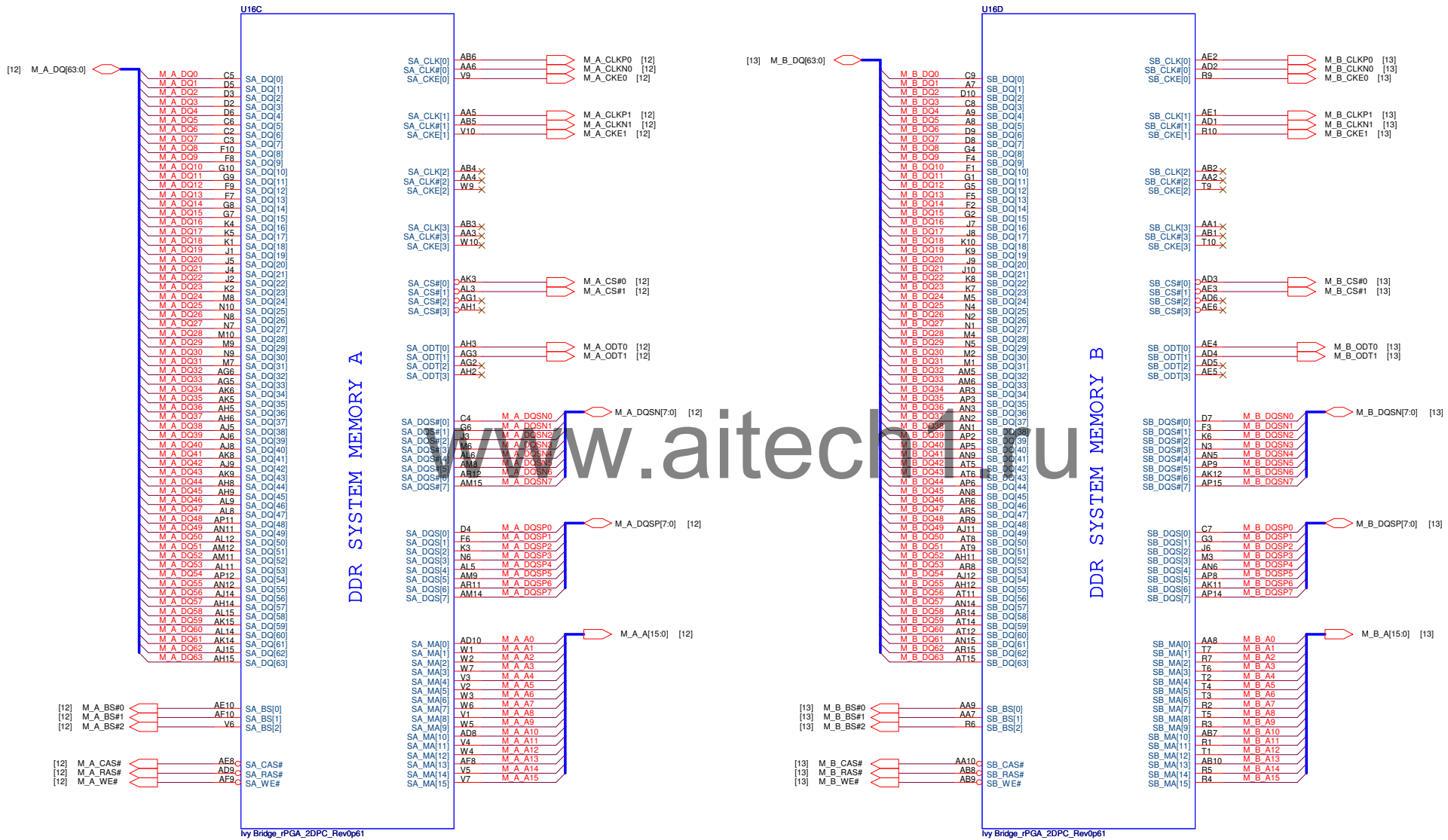
**PCH Power (+1.05/+1.8V)**

O2Micro OZ8122

DGPU Power (+VGACORE/+3.3V\_GFX/  
+1.8 VGA/+1.5 GFX/+1.05 GFX)



## Ivy Bridge Processor (DDR3)



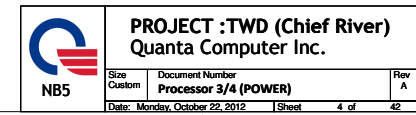
Ivy Bridge\_rPGA\_2DPC\_Rev0p61

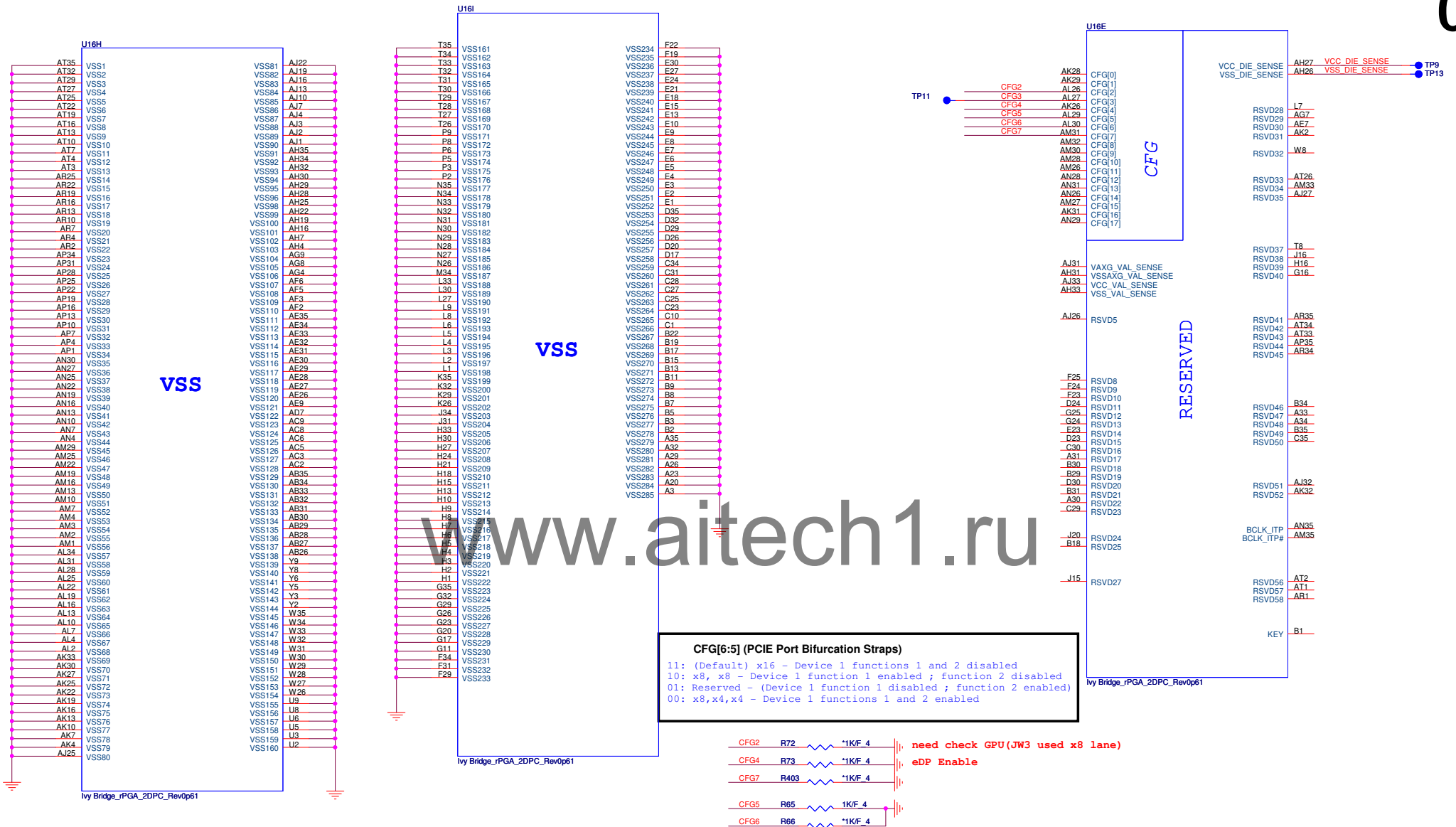
Ivy Bridge\_rPGA\_2DPC\_Rev0p61



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**Quanta Computer Inc.**

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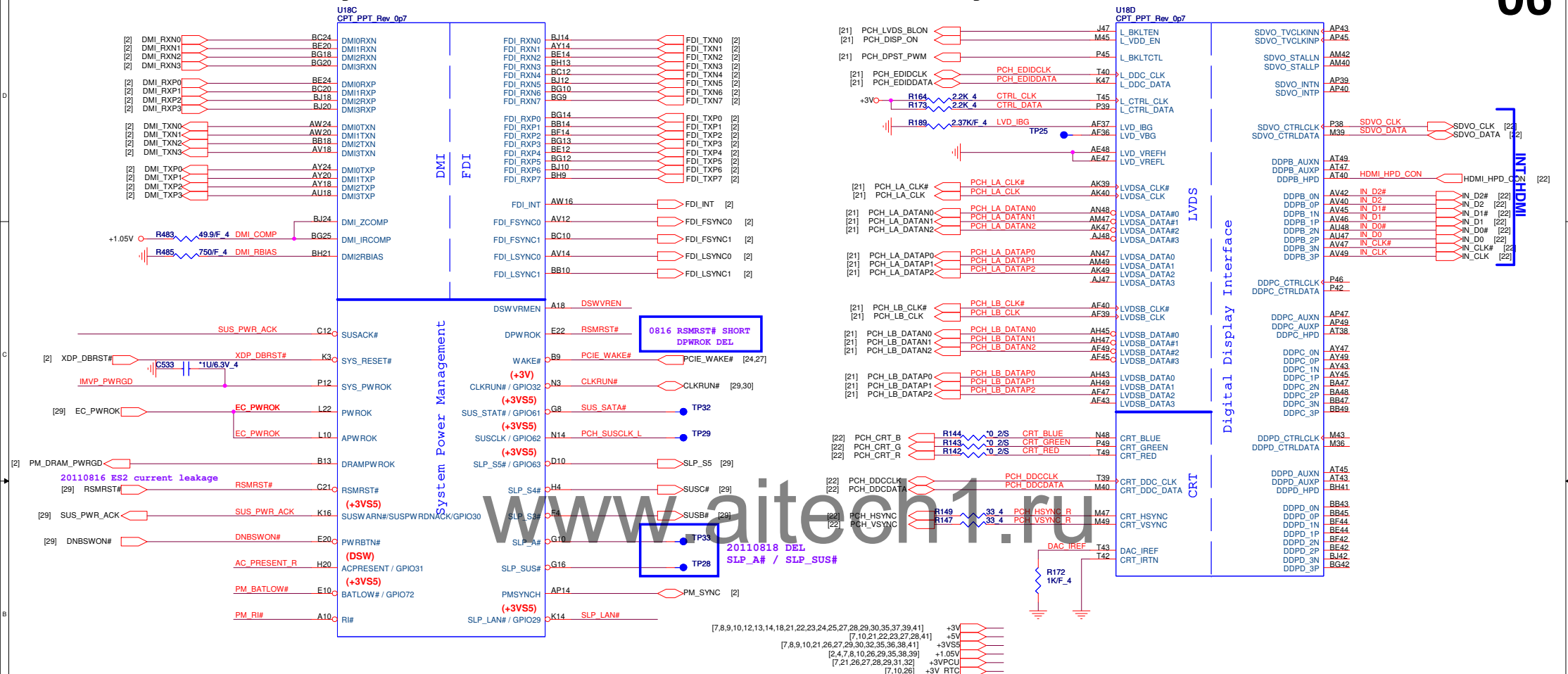




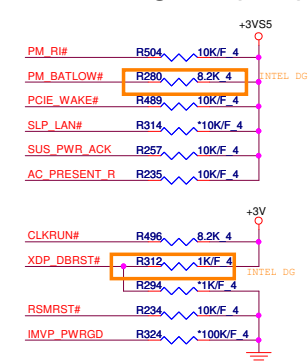
## Cougar Point/Panther Point (DMI, FDI, PM)

## Cougar Point/Panther Point (LVDS, DDI)

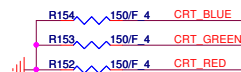
06



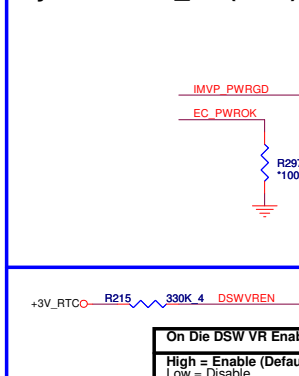
## PCH Pull-high/low(CLG)



PD Res place close to PCH

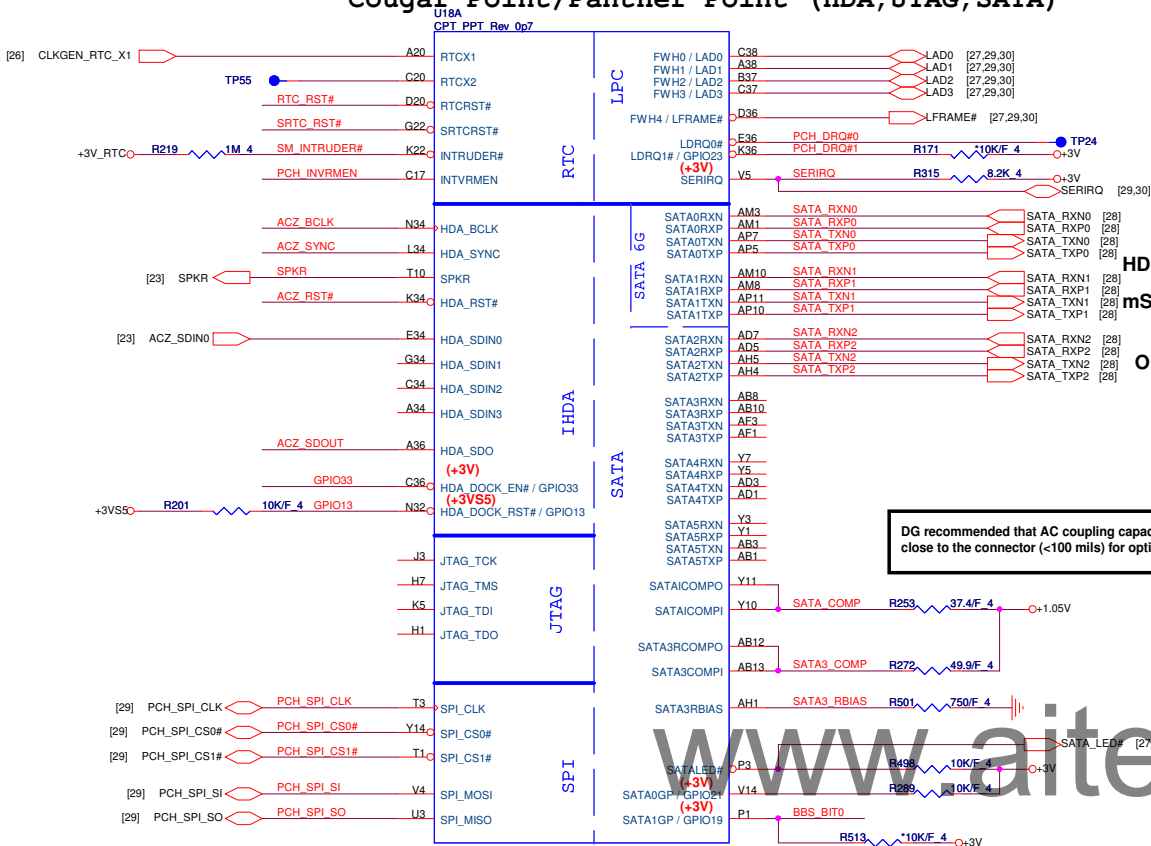
PCH to Res routing 50 ohm Impedance.  
Res to connector filter routing 37.5ohm Impedance.

## System PWR\_OK(CLG)

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## Cougar Point/Panther Point (HDA, JTAG, SATA)



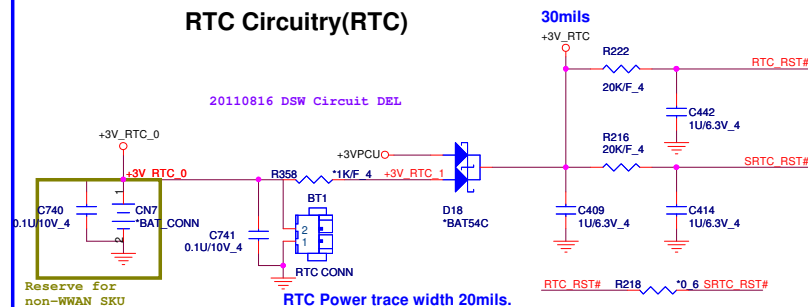
HDD0 (SATA3 6.0Gb/s)

mSATA (SATA4 3Gb/s)

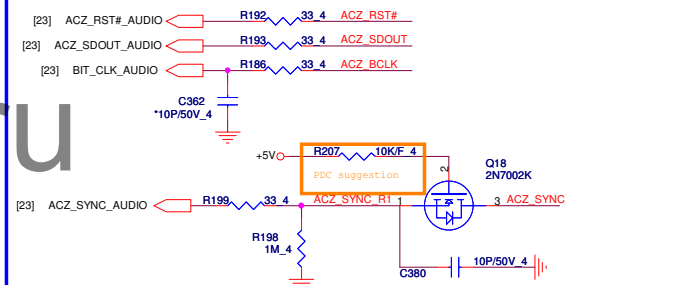
ODD (SATA2 3Gb/s)

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

## RTC Circuitry(RTC)

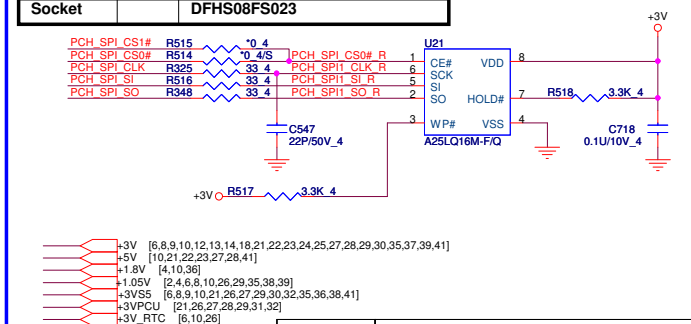


## HDA Bus(CLG)



Vender	Size	P/N
EON	2MB	AKE38ZN0Q00 (EN25QH16-104HIP)
AMIC	2MB	AKE38ZN0802 (A25LQ16M-F/Q)
Socket		DFHS08FS023

## PCH SPI ROM(CLG)



## PCH Strap Table

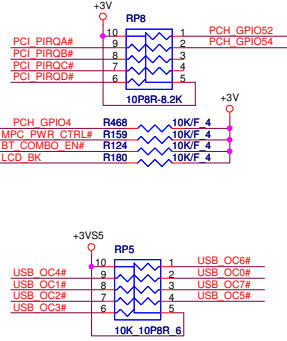
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V <sub>0</sub> R292 *1K/F 4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V <sub>0</sub> R127 *1K/F 4 PCI_GNT3# [8] +3V <sub>0</sub> R125 *1K/F 4
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V <sub>0</sub> R228 330K 4 PCH_INVRMEN
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R182 *1K/F 4 ACZ_SDOUT [29] ACZ_SDOUT
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Need external pull-down for LPC BIOS Default weak pull-up on GNT0/1#	R497 *1K/F 4 BBS_BIT0 BBS_BIT0 [8]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R132 *1K/F 4 BBS_BIT1 [8]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V <sub>0</sub> R267 *1K/F 4 INV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V <sub>0</sub> R484 2.2K 4 R482 1K/F 4 INV_CLE [9] H_SNB_IVB# [2]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VSS <sub>0</sub> R191 1K/F 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3VSS <sub>0</sub> R187 *1K/F 4 ACZ_SDOUT
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	



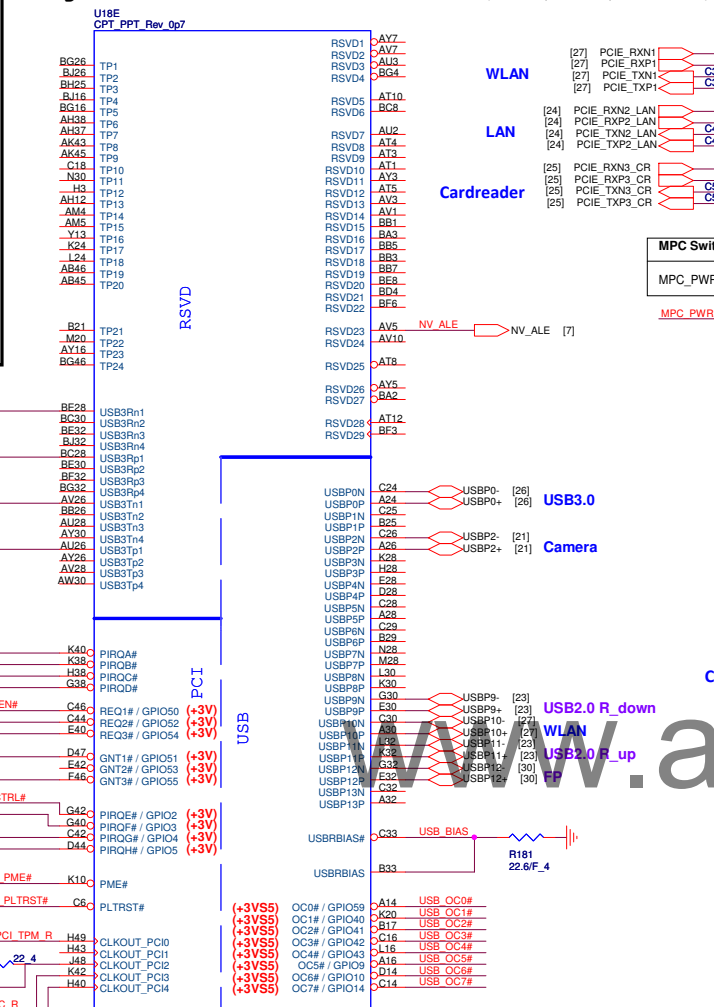
PROJECT :TWD (Chief River)  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (HDA/RTC/SATA/SPI)	A
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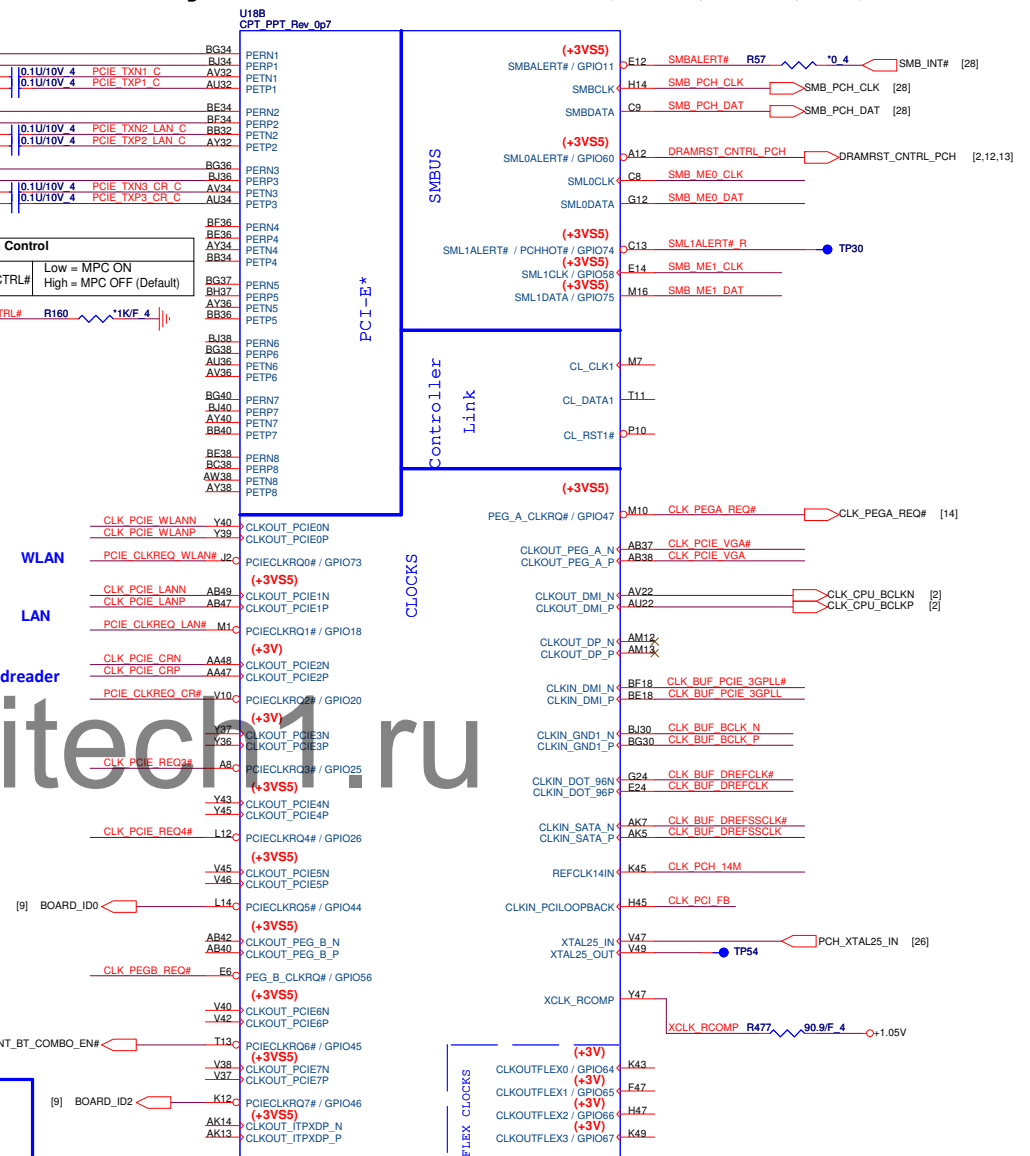
**PCI/USB OC# Pull-up (CLG)**



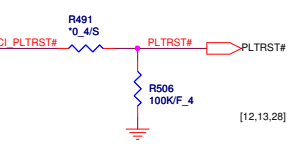
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



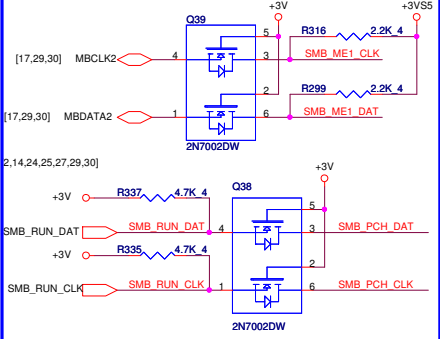
Cougar Point-M/Panther Point (PCI-E, SMBUS, CLK)



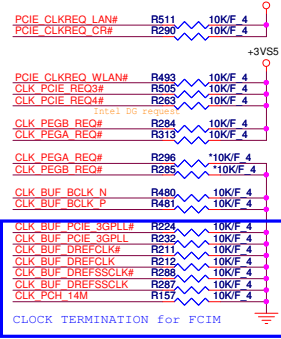
PLTRST#(CLG)



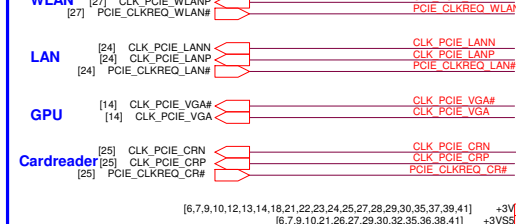
### SMBus/Pull-up(CLG)



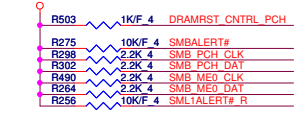
### CLK\_REQ/Strap Pin(CLG)



PCIe Clock [27]  
WLAN [23]



### SMBus/Pull-up(CLG)







+3VS5

The schematic diagram shows the I/O section of the PCB. It includes the following connections:

- SIO\_EXT\_SCS#** connected to **R183** (10K/F 4)
- SIO\_EXT\_SSW#** connected to **R499** (10K/F 4)
- BT\_OFF#** connected to **R189** (10K/F 4)
- EC\_A2GATE** connected to **R311** (10K/F 4)
- EC\_RCSIN#** connected to **R293** (10K/F 4)
- SATA5G\_P** connected to **R500** (10K/F 4)
- ODD\_PRSTNT\_#R** connected to **R499** (10K/F 4)
- DGPU\_PWROK** connected to **R174** (10K/F 4)
- DGPU\_PWROK** connected to **R175** (10K/F 4)
- GPIO27** connected to **R227** (10K/F 4)

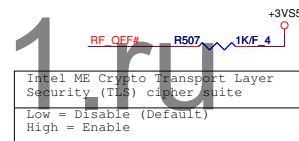
The diagram also shows a **+3V** supply and a ground connection.

BOARD_ID[3:0]	Model Name
0000	QLGA
0001	TWC
0010	JW2
0011	TBD
0100	LG3
0101	LG5
0110	LG2C
0111	LG4C
1000	TBD
1001	JW6/JW7
1010	JW3
1101	TWD

## Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO34	MODEL BIT3
BOARD_ID4	GPIO35	No Dolby=0, Dolby=1
BOARD_ID5	GPIO69	HM76=0, HM70=1
DGPU_PRSN	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

20110816 Define BRD ID[3:0]



TEST\_SET\_UP R309 10K/F 4 +3

UP
Strong (Default)

BIOS RECOVERY	High = Disable (Default) Low = Enable
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TEST DETECT
Low = Default

SATA2GP/GPIO36	Reserved only
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FDI TERMINATION VOLTAGE OVERRIDE	Reserved only
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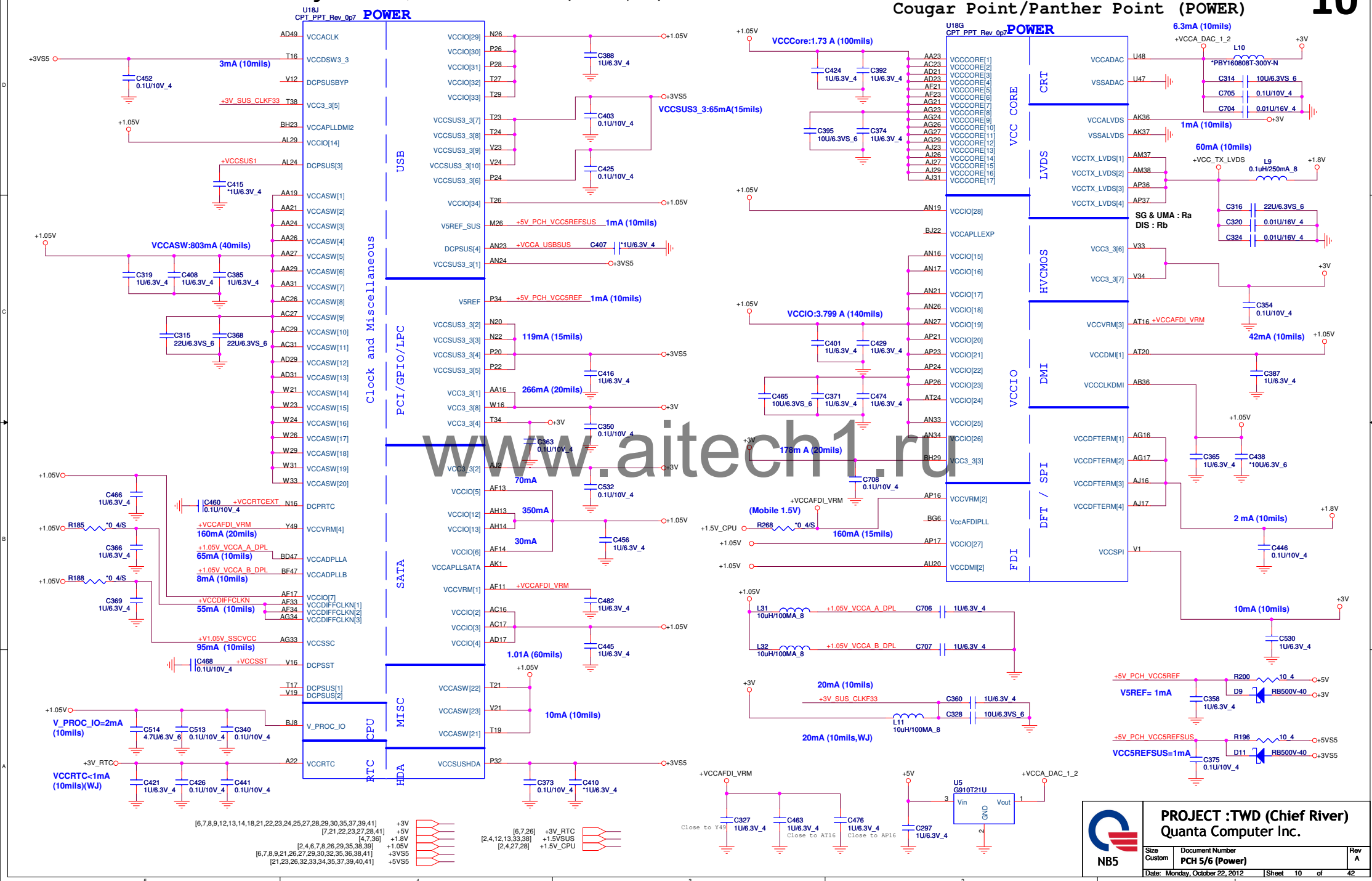
[6,7,8,10,12,13,14,18,21,22,23,24,25,27,28,29,30,35,37,39,41] +3V  
[6,7,8,10,21,26,27,29,30,32,35,36,38,41] +3VS5



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Cougar Point/Panther Point (POWER, WJ)

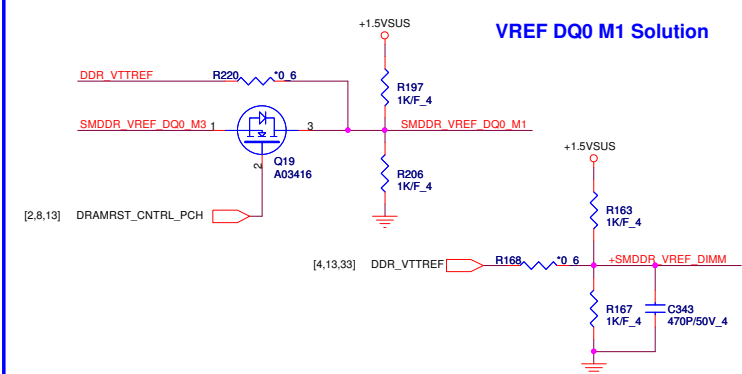
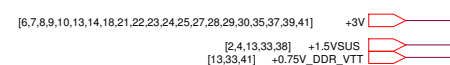


## Cougar Point/Panther Point (GND)


U18I		
CPT PPT Rev Op7		
AY4	VSS[159]	VSS[259]
AY42	VSS[160]	VSS[260]
AY46	VSS[161]	VSS[261]
AY8	VSS[162]	VSS[262]
B11	VSS[163]	VSS[263]
B12	VSS[164]	VSS[264]
B19	VSS[165]	VSS[265]
B23	VSS[166]	VSS[266]
B27	VSS[167]	VSS[267]
B31	VSS[168]	VSS[268]
B35	VSS[169]	VSS[269]
B39	VSS[170]	VSS[270]
B7	VSS[171]	VSS[271]
F45	VSS[172]	VSS[272]
BB12	VSS[173]	VSS[273]
BB16	VSS[174]	VSS[274]
BB20	VSS[175]	VSS[275]
BB22	VSS[176]	VSS[276]
BB24	VSS[177]	VSS[277]
BB28	VSS[178]	VSS[278]
BB30	VSS[179]	VSS[279]
BB38	VSS[180]	VSS[280]
BB4	VSS[181]	VSS[281]
BB46	VSS[182]	VSS[282]
RC14	VSS[183]	VSS[283]
RC18	VSS[184]	VSS[284]
BC2	VSS[185]	VSS[285]
BC22	VSS[186]	VSS[286]
BC32	VSS[187]	VSS[287]
BC38	VSS[188]	VSS[288]
BC34	VSS[189]	VSS[289]
BC36	VSS[190]	VSS[290]
BC40	VSS[191]	VSS[291]
BC42	VSS[192]	VSS[292]
BC48	VSS[193]	VSS[293]
BD46	VSS[194]	VSS[294]
BD5	VSS[195]	VSS[295]
BE22	VSS[196]	VSS[296]
BE26	VSS[197]	VSS[297]
BE40	VSS[198]	VSS[298]
BE10	VSS[199]	VSS[299]
BE12	VSS[200]	VSS[300]
BF16	VSS[201]	VSS[301]
BF20	VSS[202]	VSS[302]
BF22	VSS[203]	VSS[303]
BF24	VSS[204]	VSS[304]
BF26	VSS[205]	VSS[305]
BF28	VSS[206]	VSS[306]
BD3	VSS[207]	VSS[307]
BF40	VSS[208]	VSS[308]
BF38	VSS[209]	VSS[309]
BF40	VSS[210]	VSS[310]
BF8	VSS[211]	VSS[311]
RG17	VSS[212]	VSS[312]
RG21	VSS[213]	VSS[313]
RG33	VSS[214]	VSS[314]
RG44	VSS[215]	VSS[315]
BG8	VSS[216]	VSS[316]
BH11	VSS[217]	VSS[317]
BH15	VSS[218]	VSS[318]
BH17	VSS[219]	VSS[319]
BH19	VSS[220]	VSS[320]
H10	VSS[221]	VSS[321]
BH27	VSS[222]	VSS[322]
BH31	VSS[223]	VSS[323]
BH33	VSS[224]	VSS[324]
BH35	VSS[225]	VSS[325]
BH39	VSS[226]	VSS[326]
BH43	VSS[227]	VSS[327]
BH7	VSS[228]	VSS[328]
D3	VSS[229]	VSS[329]
D12	VSS[230]	VSS[330]
D16	VSS[231]	VSS[331]
D18	VSS[232]	VSS[332]
D22	VSS[233]	VSS[333]
D24	VSS[234]	VSS[334]
D26	VSS[235]	VSS[335]
D30	VSS[236]	VSS[336]
D32	VSS[237]	VSS[337]
D34	VSS[238]	VSS[338]
D38	VSS[239]	VSS[339]
D42	VSS[240]	VSS[340]
D8	VSS[241]	VSS[341]
E18	VSS[242]	VSS[342]
E26	VSS[243]	VSS[343]
G18	VSS[244]	VSS[344]
G20	VSS[245]	VSS[345]
G26	VSS[246]	VSS[346]
G28	VSS[247]	VSS[347]
G36	VSS[248]	VSS[348]
G48	VSS[249]	VSS[349]
H12	VSS[250]	VSS[350]
H18	VSS[251]	VSS[351]
H22	VSS[252]	VSS[352]
H24	VSS[253]	VSS[353]
H26	VSS[254]	VSS[354]
H30	VSS[255]	VSS[355]
H32	VSS[256]	VSS[356]
H34	VSS[257]	VSS[357]
F3	VSS[258]	VSS[358]

## Cougar Point/Panther Point (GND)

U18H		
CPT PPT Rev Op7		
H5	VSS[0]	
AA17	VSS[1]	VSS[80]
AA2	VSS[2]	VSS[81]
AA3	VSS[3]	VSS[82]
AA33	VSS[4]	VSS[83]
AA34	VSS[5]	VSS[84]
AB11	VSS[6]	VSS[85]
AB14	VSS[7]	VSS[86]
AB39	VSS[8]	VSS[87]
AB4	VSS[9]	VSS[88]
AB43	VSS[10]	VSS[89]
P16	VSS[11]	VSS[90]
AB7	VSS[12]	VSS[91]
AC19	VSS[13]	VSS[92]
AC2	VSS[14]	VSS[93]
AC21	VSS[15]	VSS[94]
AC24	VSS[16]	VSS[95]
AC33	VSS[17]	VSS[96]
AC34	VSS[18]	VSS[97]
AC48	VSS[19]	VSS[98]
AD10	VSS[20]	VSS[99]
AD11	VSS[21]	VSS[100]
AD12	VSS[22]	VSS[101]
AD13	VSS[23]	VSS[102]
AD19	VSS[24]	VSS[103]
AD24	VSS[25]	VSS[104]
AD26	VSS[26]	VSS[105]
AD27	VSS[27]	VSS[106]
AD33	VSS[28]	VSS[107]
AD34	VSS[29]	VSS[108]
AD36	VSS[30]	VSS[109]
AD37	VSS[31]	VSS[110]
AD38	VSS[32]	VSS[111]
AD39	VSS[33]	VSS[112]
AD4	VSS[34]	VSS[113]
AD40	VSS[35]	VSS[114]
AD42	VSS[36]	VSS[115]
AD43	VSS[37]	VSS[116]
AD45	VSS[38]	VSS[117]
AD46	VSS[39]	VSS[118]
AD8	VSS[40]	VSS[119]
AE2	VSS[41]	VSS[120]
AE3	VSS[42]	VSS[121]
AF10	VSS[43]	VSS[122]
AF12	VSS[44]	VSS[123]
AD14	VSS[45]	VSS[124]
AD16	VSS[46]	VSS[125]
AF18	VSS[47]	VSS[126]
AF19	VSS[48]	VSS[127]
AF24	VSS[49]	VSS[128]
AF29	VSS[50]	VSS[129]
AF3	VSS[51]	VSS[130]
AF38	VSS[52]	VSS[131]
AF39	VSS[53]	VSS[132]
AF4	VSS[54]	VSS[133]
AF42	VSS[55]	VSS[134]
AF46	VSS[56]	VSS[135]
AF5	VSS[57]	VSS[136]
AF7	VSS[58]	VSS[137]
AF8	VSS[59]	VSS[138]
AG19	VSS[60]	VSS[139]
AG2	VSS[61]	VSS[140]
AG31	VSS[62]	VSS[141]
AG31	VSS[63]	VSS[142]
AG48	VSS[64]	VSS[143]
AH11	VSS[65]	VSS[144]
AH3	VSS[66]	VSS[145]
AH36	VSS[67]	VSS[146]
AH39	VSS[68]	VSS[147]
AH40	VSS[69]	VSS[148]
AH42	VSS[70]	VSS[149]
AH46	VSS[71]	VSS[150]
AH7	VSS[72]	VSS[151]
AJ19	VSS[73]	VSS[152]
AJ21	VSS[74]	VSS[153]
AJ24	VSS[75]	VSS[154]
AJ33	VSS[76]	VSS[155]
AJ4	VSS[77]	VSS[156]
AK12	VSS[78]	VSS[157]
AK3	VSS[79]	VSS[158]
AK38		VSS[80]
AK4		VSS[81]
AK42		VSS[82]
AK46		VSS[83]
AK8		VSS[84]
AL16		VSS[85]
AL17		VSS[86]
AL19		VSS[87]
AL2		VSS[88]
AL21		VSS[89]
AL23		VSS[90]
AL28		VSS[91]
AL27		VSS[92]
AL31		VSS[93]
AL33		VSS[94]
AL34		VSS[95]
AL48		VSS[96]
AM11		VSS[97]
AM14		VSS[98]
AM36		VSS[99]
AM39		VSS[100]
AM43		VSS[101]
AM45		VSS[102]
AM46		VSS[103]
AM7		VSS[104]
AN2		VSS[105]
AN29		VSS[106]
AN31		VSS[107]
AP12		VSS[108]
AP19		VSS[109]
AP28		VSS[110]
AP30		VSS[111]
AP32		VSS[112]
AP38		VSS[113]
AP4		VSS[114]
AP42		VSS[115]
AP46		VSS[116]
AP8		VSS[117]
AR2		VSS[118]
AR48		VSS[119]
AT11		VSS[120]
AT13		VSS[121]
AT18		VSS[122]
AT22		VSS[123]
AT26		VSS[124]
AT32		VSS[125]
AT34		VSS[126]
AT39		VSS[127]
AT42		VSS[128]
AT46		VSS[129]
AT7		VSS[130]
AU24		VSS[131]
AU30		VSS[132]
AV16		VSS[133]
AV20		VSS[134]
AV24		VSS[135]
AV30		VSS[136]
AV38		VSS[137]
AV4		VSS[138]
AV43		VSS[139]
AV8		VSS[140]
AW14		VSS[141]
AW18		VSS[142]
AW2		VSS[143]
AW22		VSS[144]
AW26		VSS[145]
AW28		VSS[146]
AW32		VSS[147]
AW34		VSS[148]
AW36		VSS[149]
AW40		VSS[150]
AW48		VSS[151]
AV11		VSS[152]
AV12		VSS[153]
AY22		VSS[154]
AY28		VSS[155]
AY28		VSS[156]
AY28		VSS[157]
AY28		VSS[158]





 NB5	<b>PROJECT :TWD (Chief River)</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>System Memory 2/2 (9.2H)</b>	Rev A
	Date: Monday, October 22, 2012	Sheet 13 of 42	



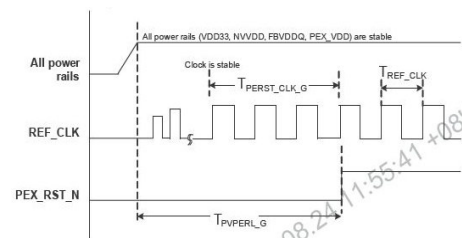
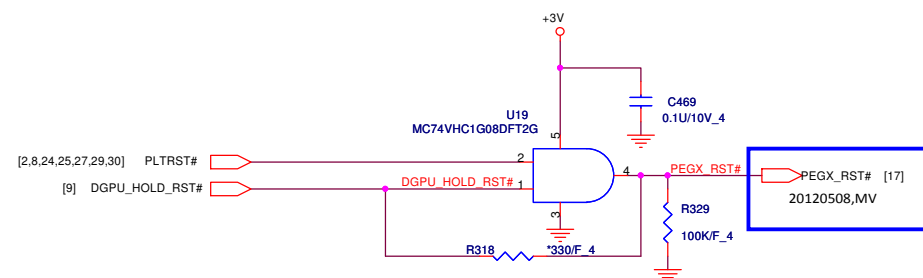
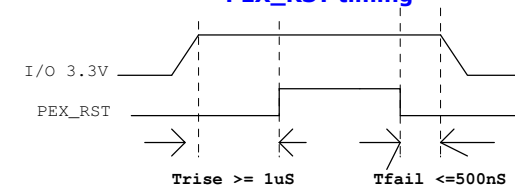
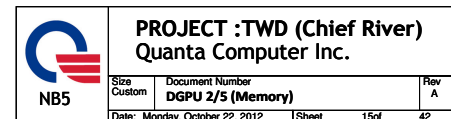


Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T <sub>FVPERL_G</sub>	T <sub>FVPERL_G</sub> ≥ 103	
T <sub>FPERST_CLK_G</sub>	T <sub>FPERST_CLK_G</sub> ≥ 1T <sub>REF_CLK</sub>	

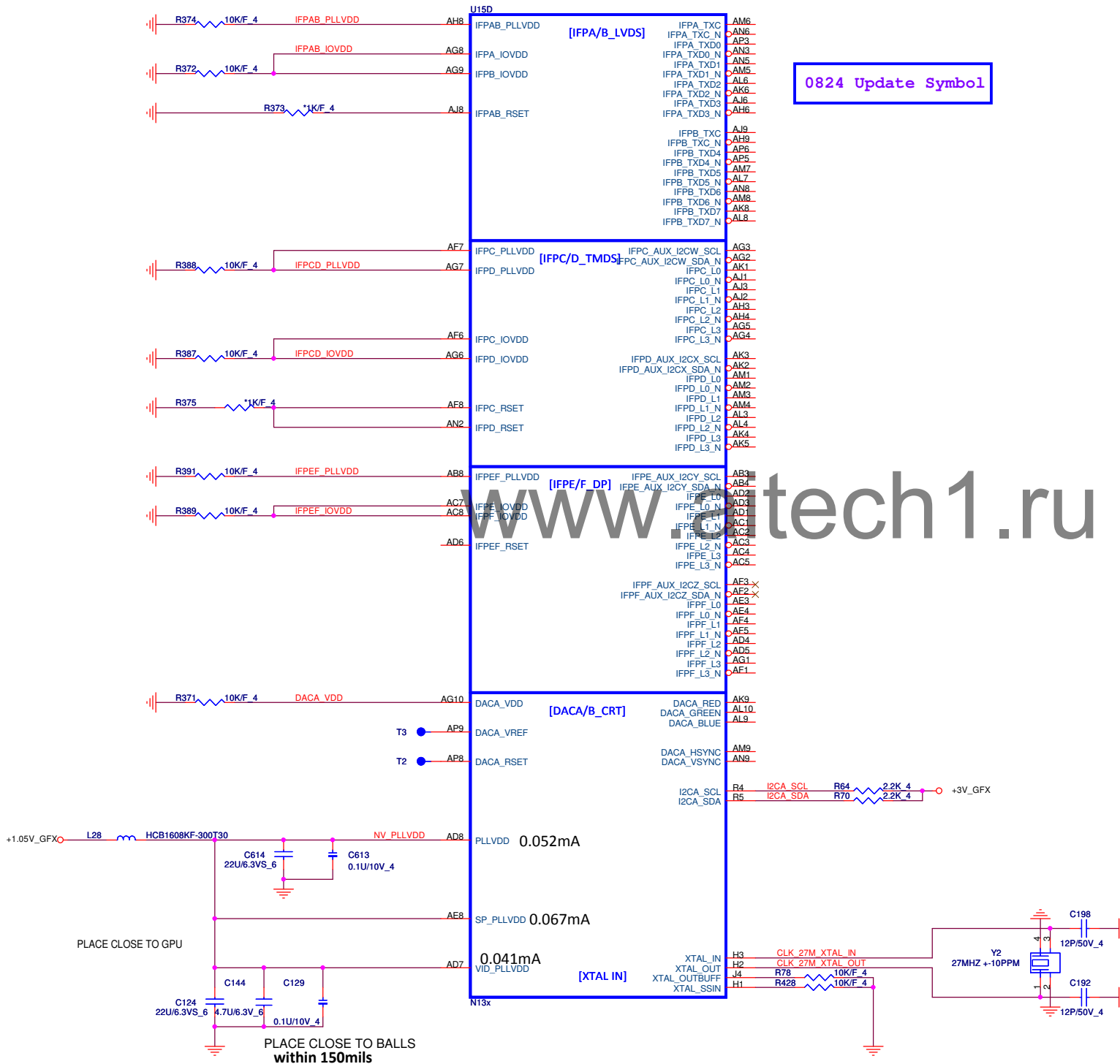
## PEX\_RST timing





[14,15,18,38] +1.05V\_GFX  
[14,17,18,37,38] +3V\_GFX

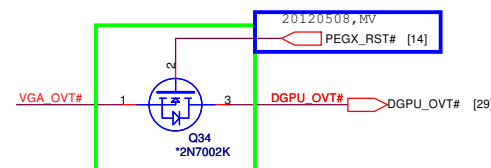
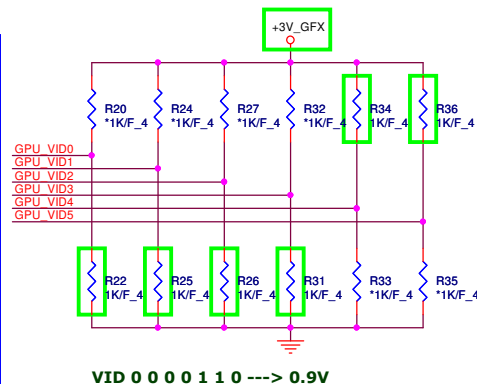
0824 Update Symbol



**PROJECT :TWD (Chief River)**  
**Quanta Computer Inc.**

Size A3	Document Number DGPU 3/5 (Display)	Rev A
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Net name	N13P-GLR	N13P-GSR
ROM_SI		
ROM_SO	PD 10K	PU 10K
ROM_SCLK	PD 15K	PU 5K
STRAP0	PU 45K	PU 45K
STRAP1	PD 45K	PD 5K
STRAP2	PD 20K	PU 10K
STRAP3	UN-STUFF	PD 5K
STRAP4	UN-STUFF	PD 45K



For N13P-GLR  
ROM\_SO PD 10K  
ROM\_SCLK PD 15K

N13P-GLR ID:0xDe3  
N13P-GSR ID:0xDF9

### Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Default: Samsung 2G VRAM

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	1001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0011
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0111
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	XXXX
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	XXXX

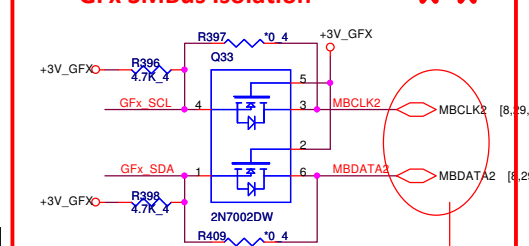
For N13P-GLR N13P-GSR  
Default : 2G Samsung  
VRAM Configuration Table

ROM\_SI  
1G Hynix 64Mx16 (D-Die) -->15K PD  
1G Samsung 64Mx16(G-Die)-->20K PD  
2G Hynix 128Mx16 (D-Die) -->30K PD  
2G Samsung 128Mx16 E-die  
N13P-GLR -->10K PD  
N13P-GSR -->25K PD

### GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

### GFx SMBus Isolation

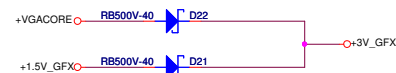


N13P-GLR	N13P-GSR
Stuff Rc	Un-stuff Rc

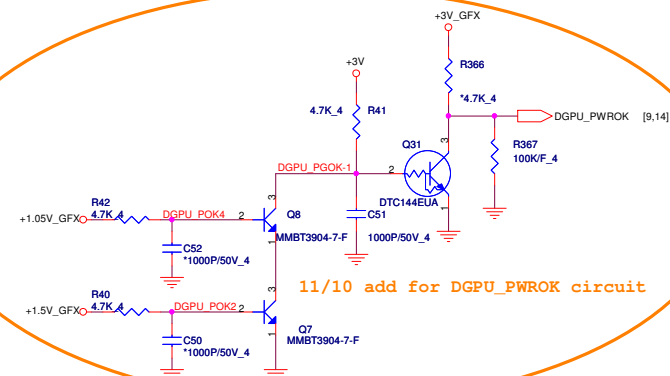
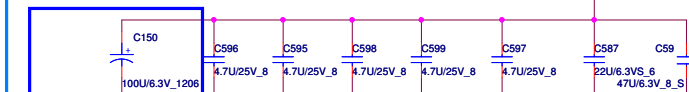


PROJECT :TWD (Chief River)  
Quanta Computer Inc.

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## Place to GPU Center





```
[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]
```






```

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

```



```

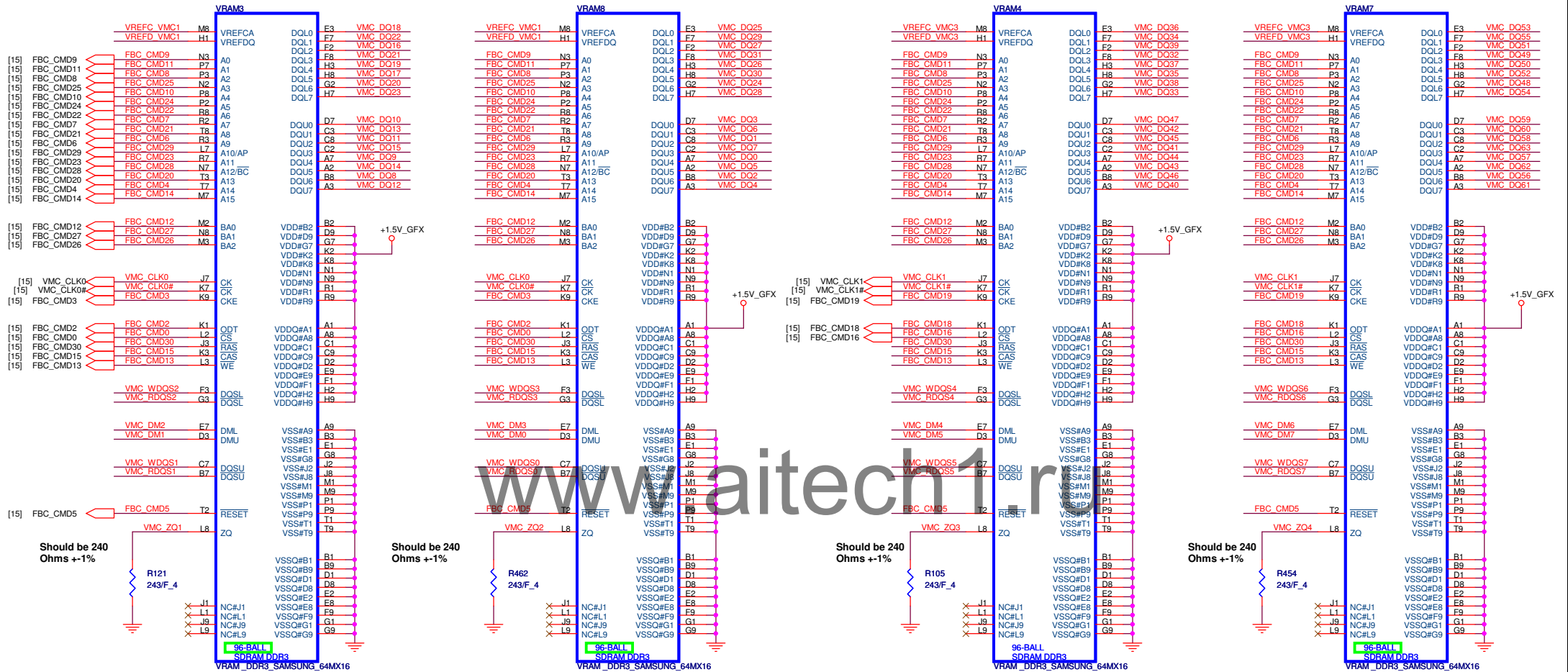
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)
  
```



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[15] VMC\_DQ[63..0]  
[15] VMC\_DM[7..0]  
[15] VMC\_WDQS[7..0]  
[15] VMC\_RDQS[7..0]

# CHANNEL B: 256MB/512MB DDR3



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VMC\_CLK0  
R451  
162/F\_4  
VMC\_CLK0#

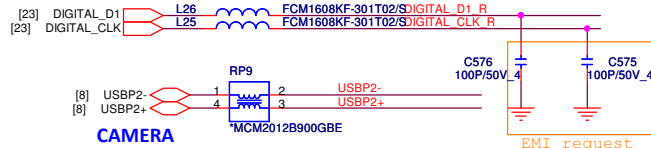
Fermi : Change to 160 ohm (WJ)  
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)  
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)

VMC\_CLK1  
R108  
162/F\_4  
VMC\_CLK1#

Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)  
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)

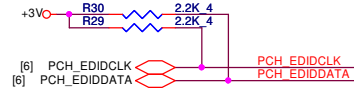
# USB Camera Connector

## MIC

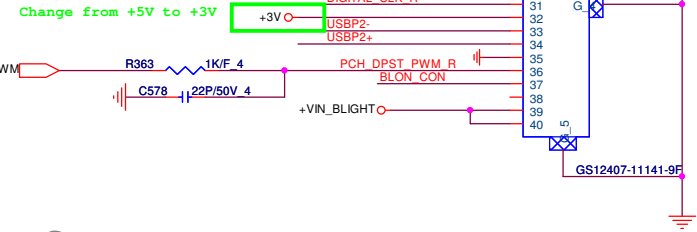


8/27 B stage:del RP9

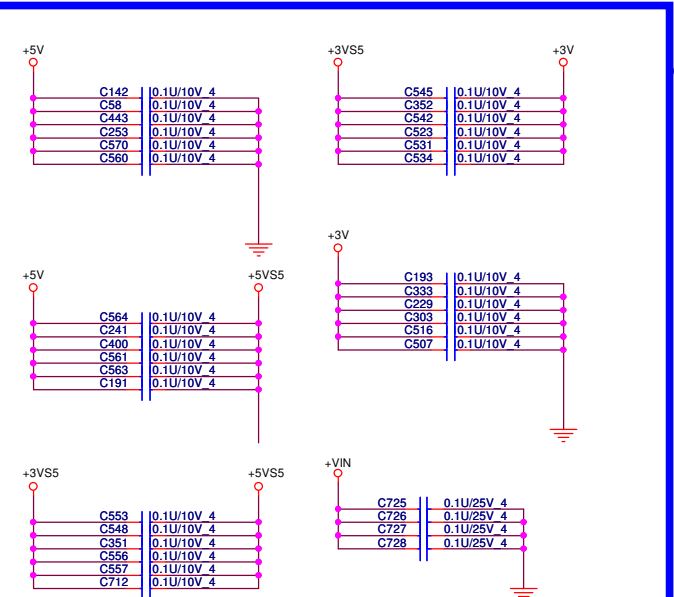
Change from +5V to +3V



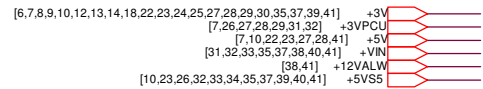
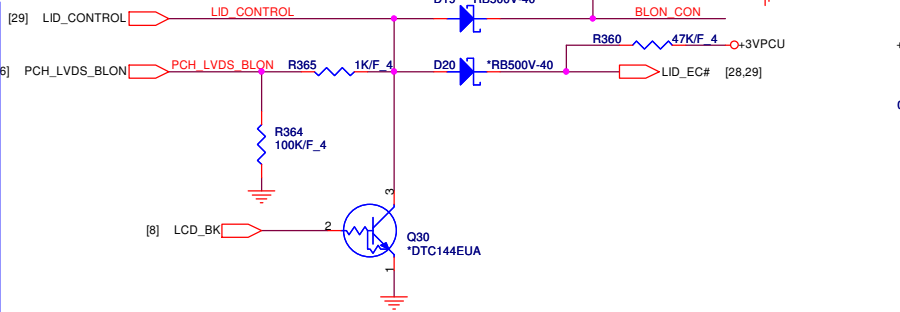
Change from +5V to +3V



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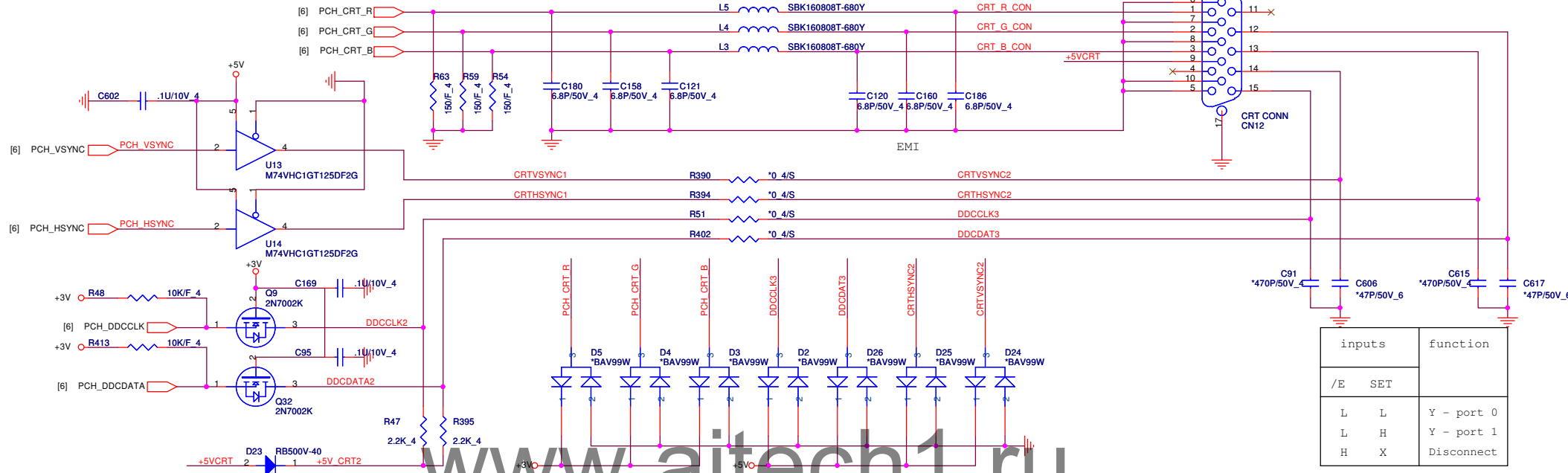
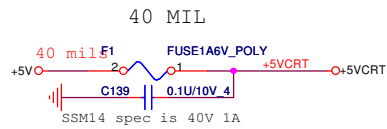


EMI/ESD  
Stitching Cap(each 1" place one cap)

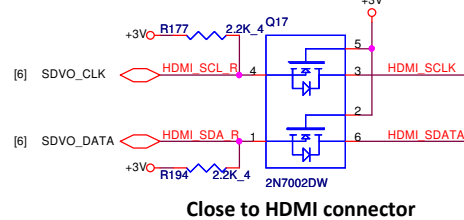


## CRT PORT

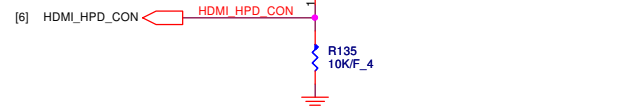
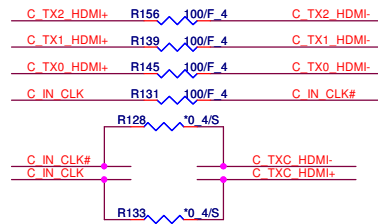
8/24 B stage:change CRT conn PN from "DFDS15FR176"to "DFDS15FR261" for ID



## HDMI SMBus Isolation

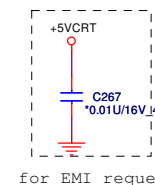
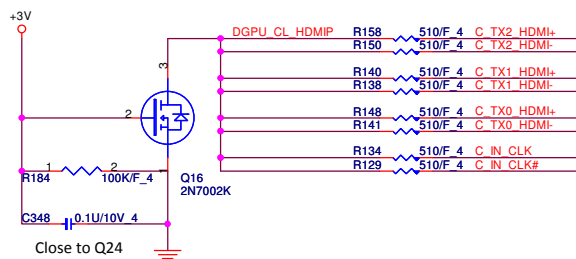
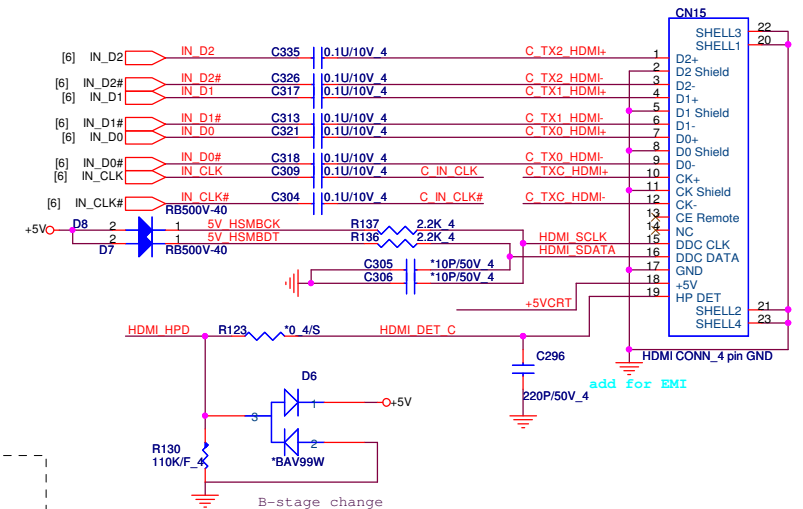


## EMI Solution



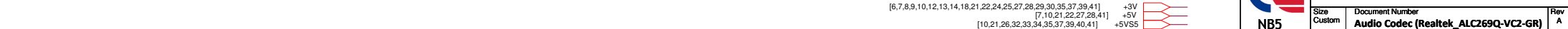
## HDMI PORT

8/24 B stage:change CRT conn PN from "DFHD19MR190"to "DFHD19MR280" for ID

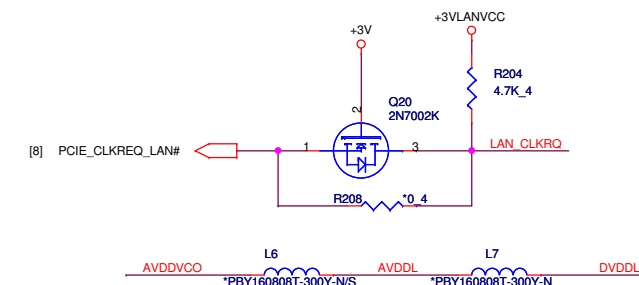


**PROJECT :TWD (Chief River)**  
**Quanta Computer Inc.**

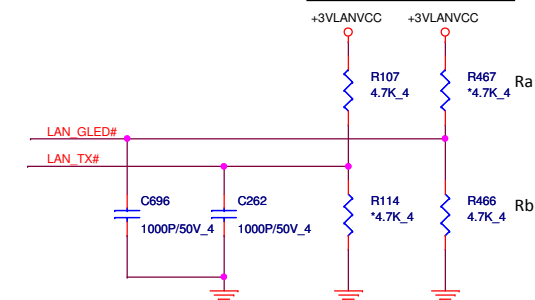
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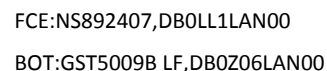


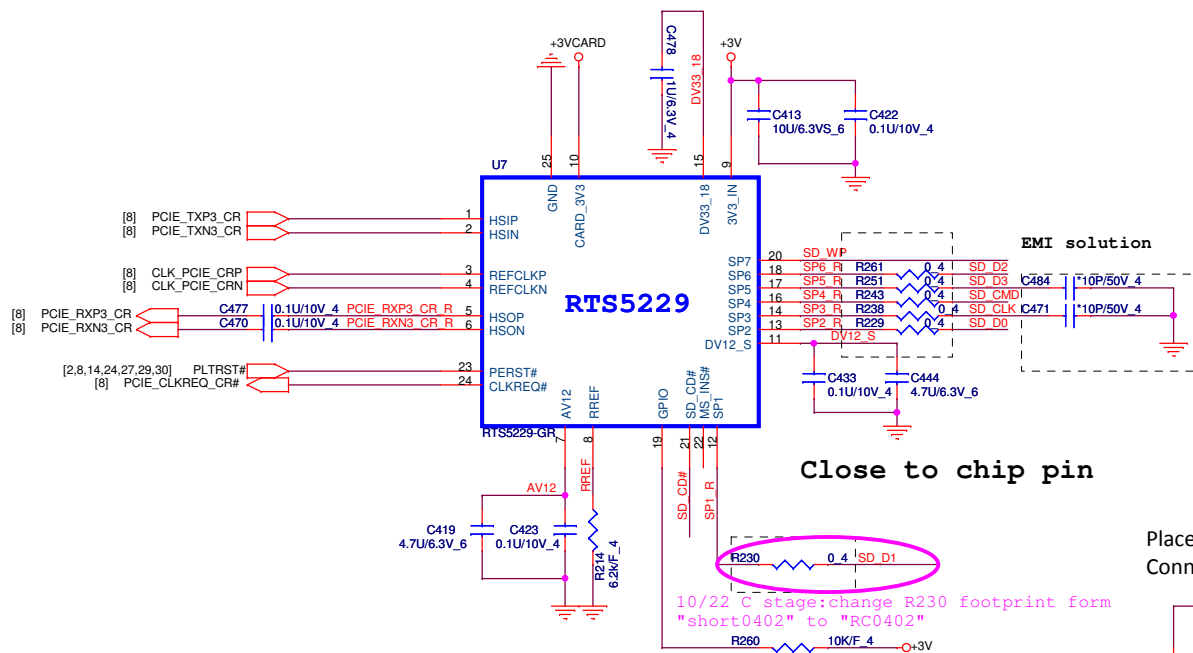


Rb(R5208)	<b>Stuff</b>
L5006	No stuff
L5004	No stuff
C5291	No stuff
C5293.	No stuff
C5294	No stuff
Ra(R5210)	No stuff

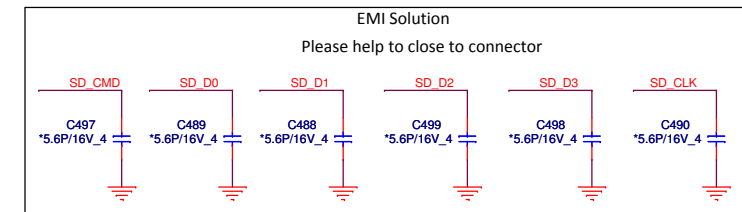


The diagram illustrates the pin configuration for the LAN interface. It shows the connection of LAN\_TX# and LAN\_GLED# signals to the RJ45 connector pins. LAN\_TX# is connected to pins 1, 2, 3, and 4. LAN\_GLED# is connected to pins 5, 6, 7, and 8. The RJ45 connector is labeled RJ45\_CONN and has pins 1 through 12. The LAN\_TX# signal is connected to pins 1, 2, 3, and 4. The LAN\_GLED# signal is connected to pins 5, 6, 7, and 8. The RJ45 connector is also connected to a +3VLANVCC supply and a GND1 ground.



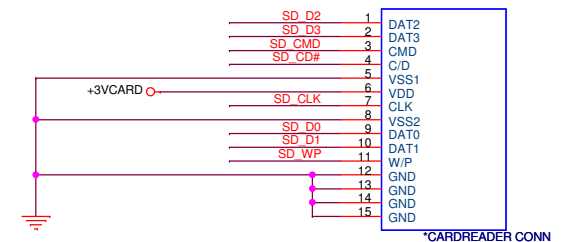


## Share Pin

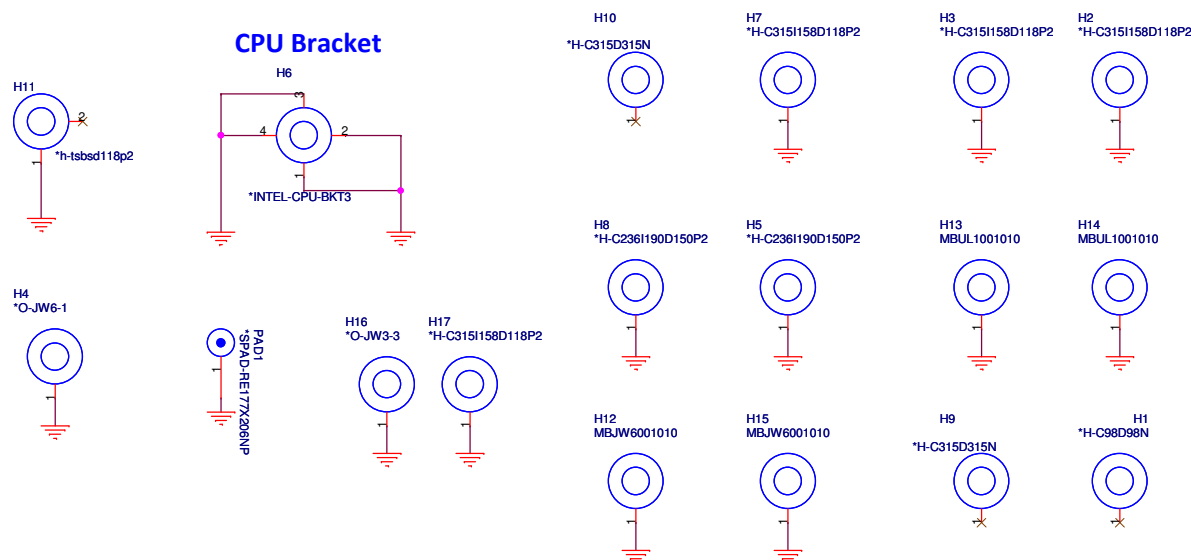


**14" ONLY SD / MMC CARD READER**

CN8

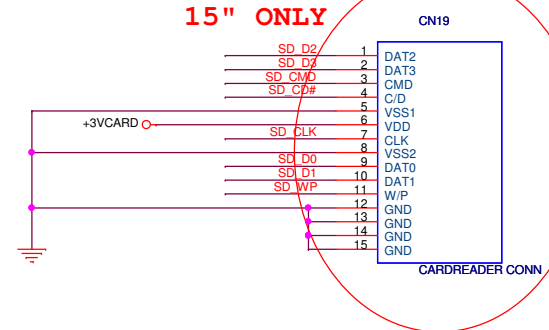


## CPU Bracket



20120614: Co-layer for 15" panel of JW3

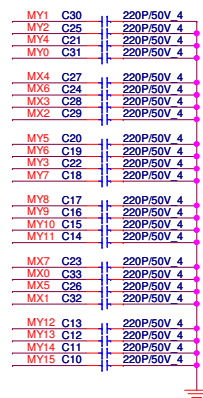
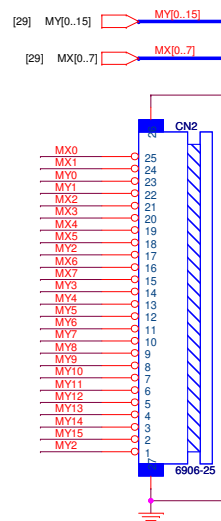
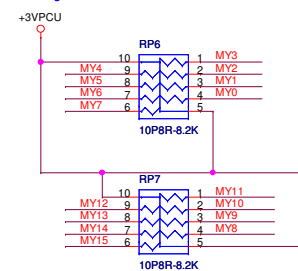
## 15" ONLY



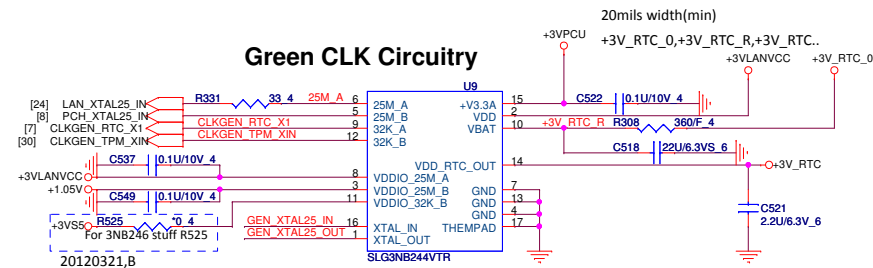
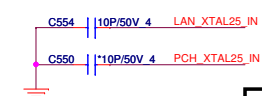
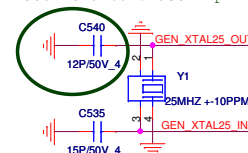
	<b>PROJECT :TWD (Chief River)</b>		
	<b>Quanta Computer Inc.</b>		
	Size Custom	Document Number	Rev A
		<b>Card Reader control (RT55229-GR)</b>	
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9/3 B stage:change R308 value form "330" to "360" for safety issue.

## Keyboard Connector



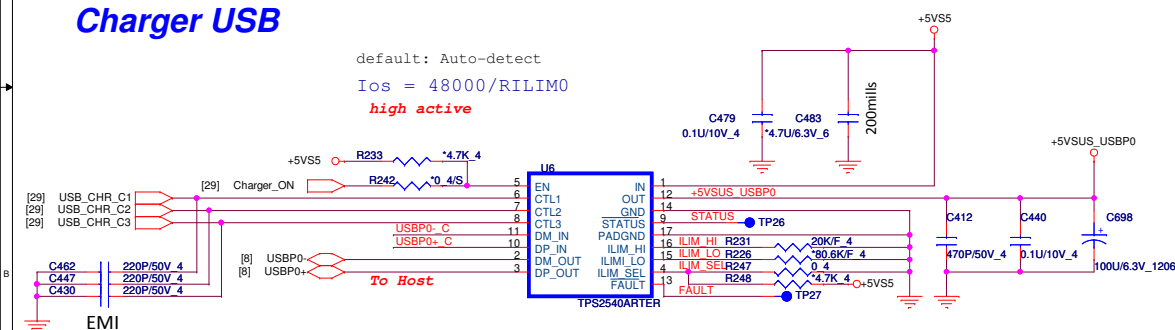
## Green CLK Circuitry

8/27 B stage:change C540 value form "15p" to "12p" for RTC issue.  
vendor recommend C540 use 12p

FOR TPM option

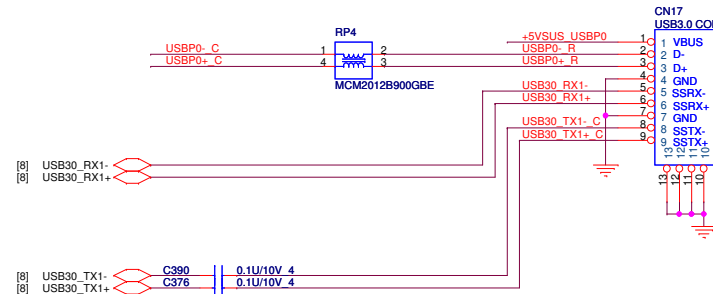
	TPM	Non-TPM
R525	Stuff	NA
U5	AL3NB246000	AL3NB244000

## Charger USB

default: Auto-detect  
Ios = 48000/RILIMO  
high active

## USB3.0 X 1/USB2.0 COMBO

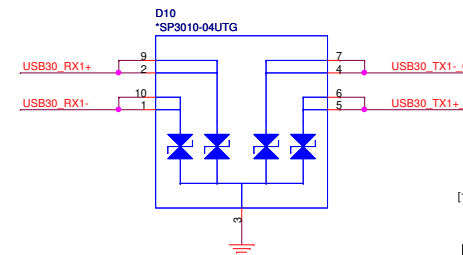
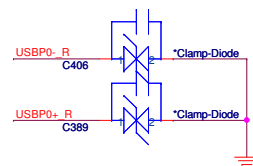
## USB 3.0



TPS2543/45 Control Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
0	0	0	1	Discharge	NA	off
0	0	1	1	DCP/auto	IOS_PW & ILIM_HI (1)	DCP load present
0	1	0	1	SDP	ILIM_HI	off
0	1	1	1	DCP/auto	ILIM_HI	DCP load present
1	1	0	1	SDP	ILIM_HI	off
1	1	1	1	CDP	ILIM_HI	CDP load present

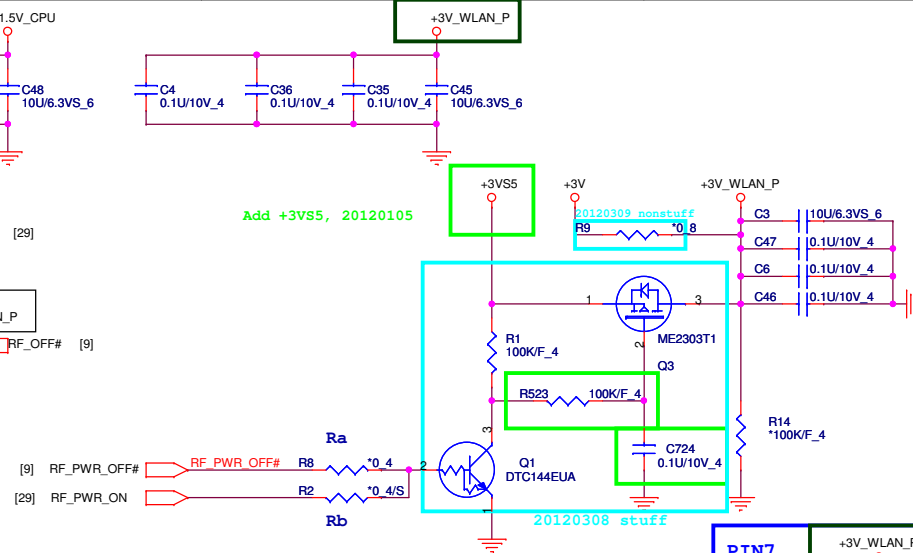
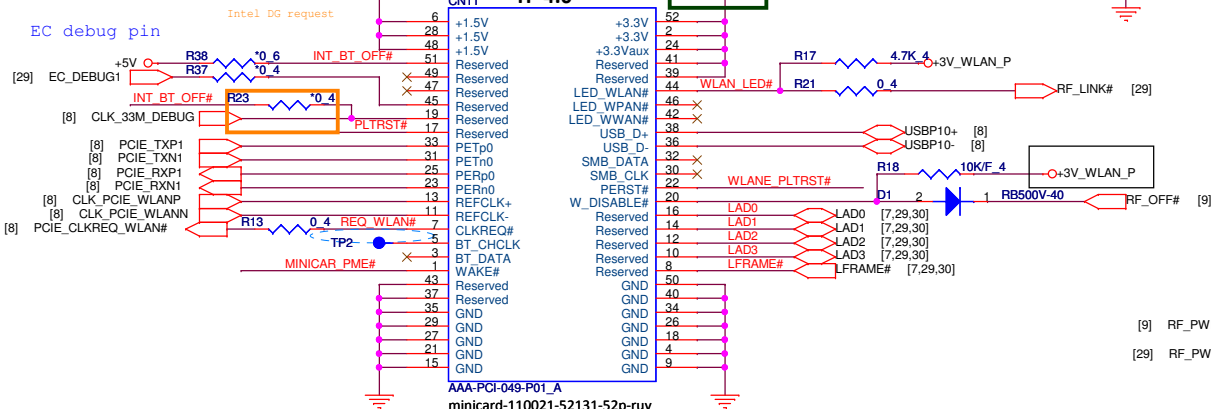
(1) ILIM\_HI: 20K(R5233), 2.4A

[10,21,23,32,33,34,35,37,39,40,41]  
[7,21,27,28,29,31,32] +5VS5  
+3VPCUPROJECT :TWD (Chief River)  
Quanta Computer Inc.

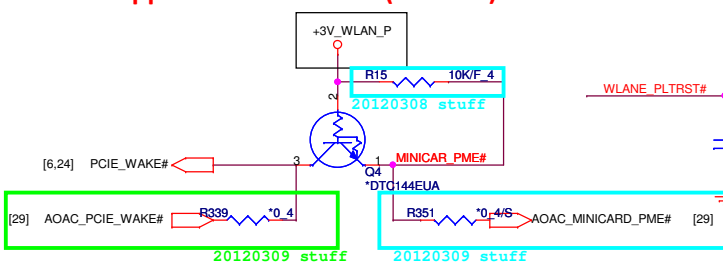
Size	Document Number	Rev
Custom	USB 3.0/KB/Green CLK	A
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**Mini Card  
WLAN/BT(Optional)**

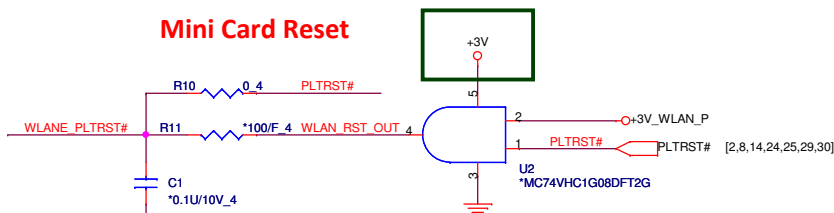
EC debug pin



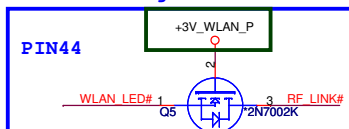
## Support Wake Function(Reserve)



## Mini Card Reset



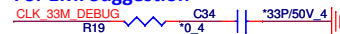
### Avoid leakage issue



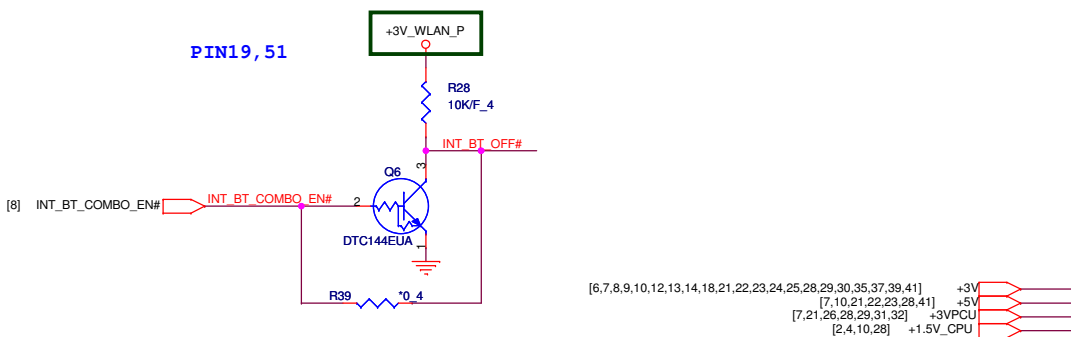
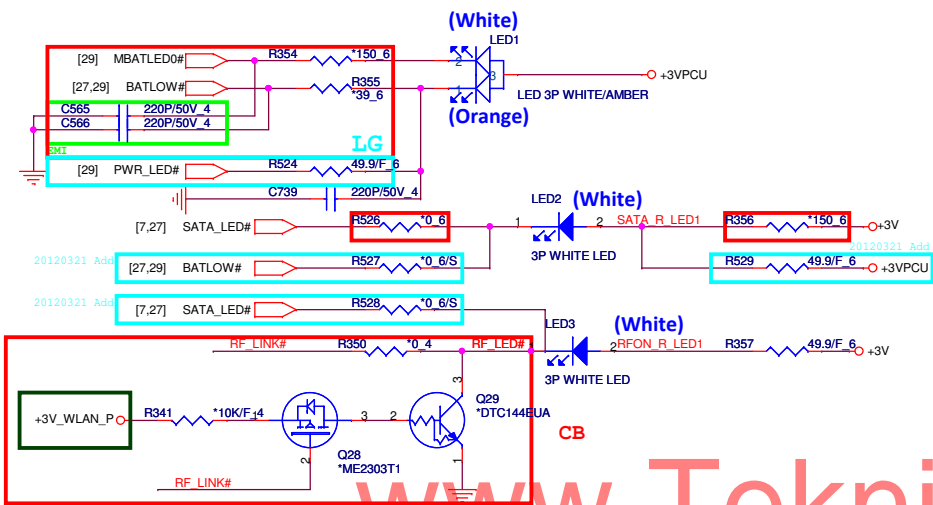
## LGE mini-pcie power status

WLAN	Bluetooth	+3V_WLAN
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

### For EMI Suggestion



## LED Status



### 9/4 Intel COMBO card control circuit

- 1.add R1001,R1002,Q1001
- 2.add net name"INT BT COMBO EN#" -> "INT BT OFF#"

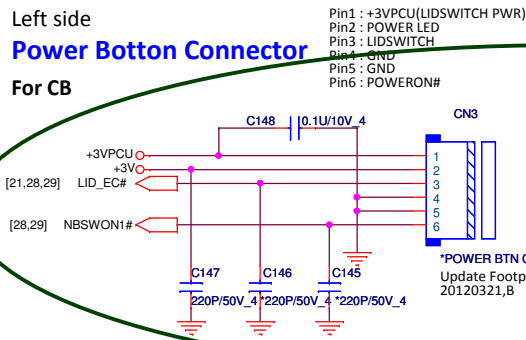


**PROJECT :TWD (Chief River)**  
Quanta Computer Inc.

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## Left side Power Button Connector

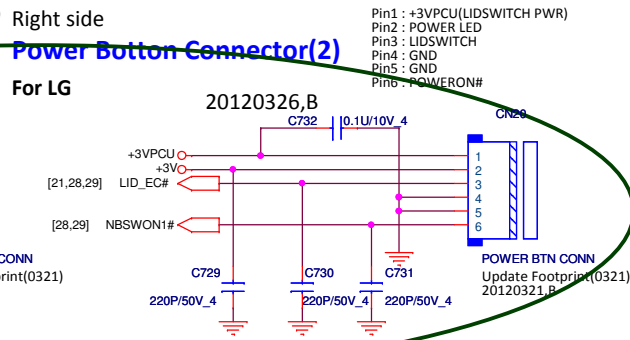
For CB



Right side

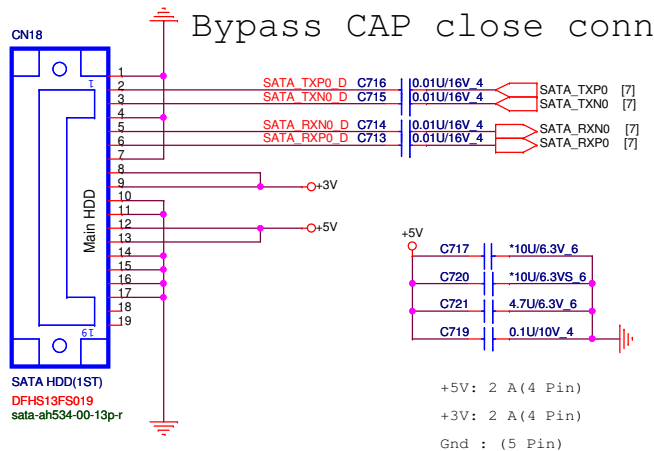
## Power Button Connector(2)

For LG

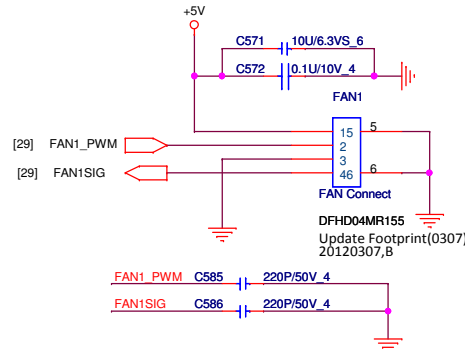


8/24 B stage:del CN3/C145/C146, add CN20/C729~C732 for change power conn location (machine ID)

## SATA HDD Connector(Cable type)

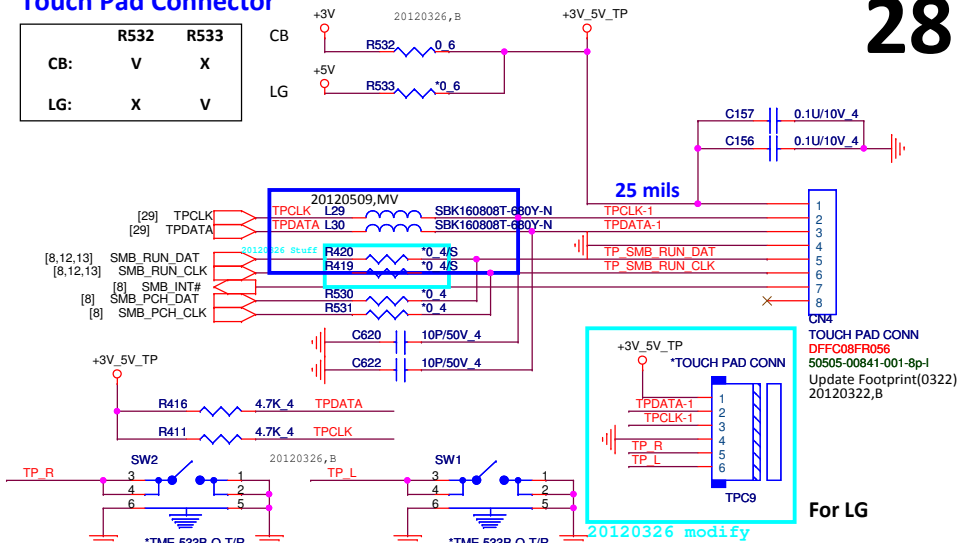


## CPU FAN

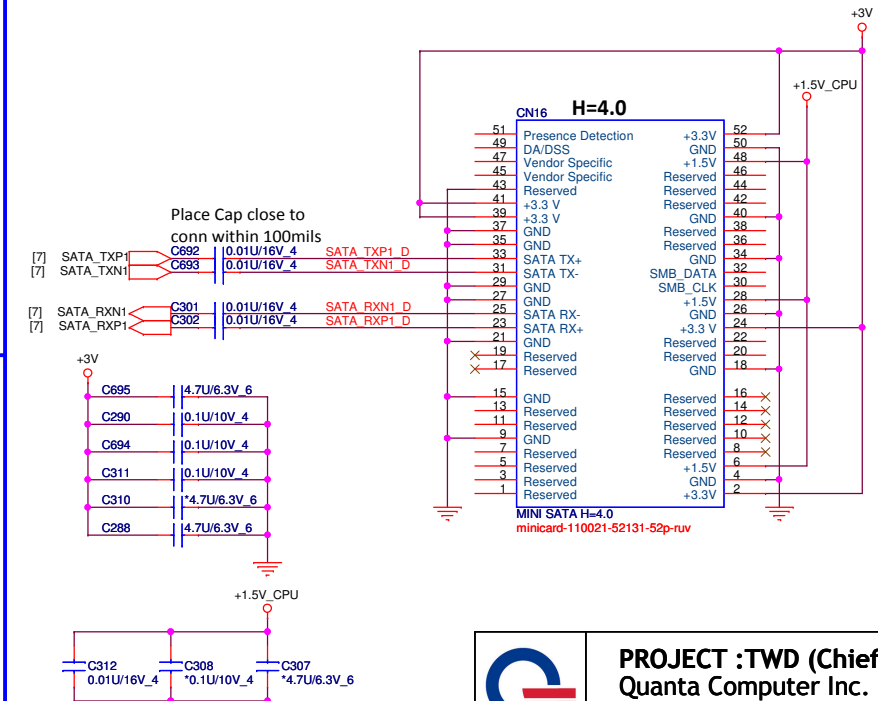


## Touch Pad Connector

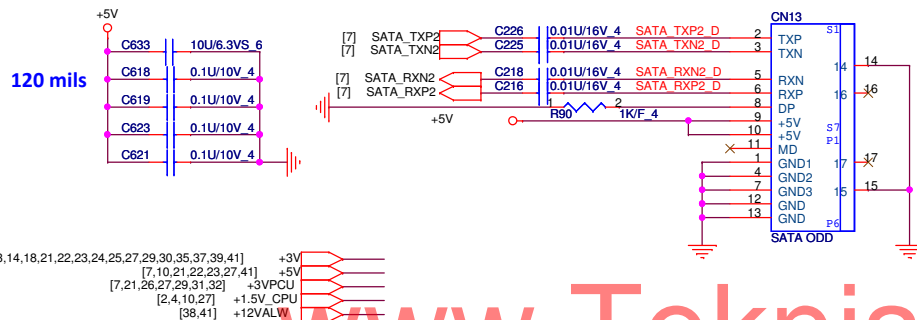
	R532	R533
CB:	V	X
LG:	X	V



## Mini PCI-E Card 2- Full size MINISATA



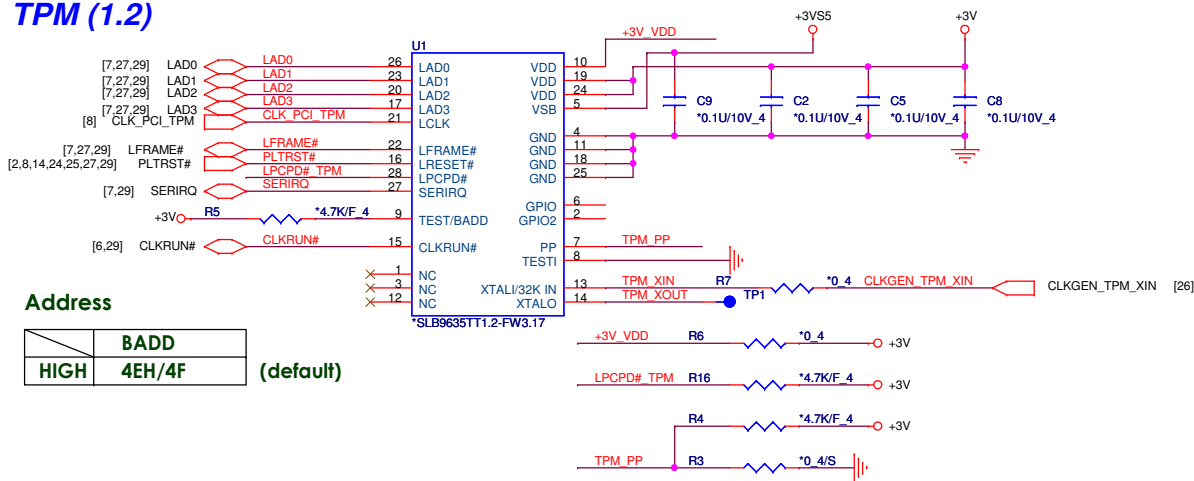
## SATA ODD Connector



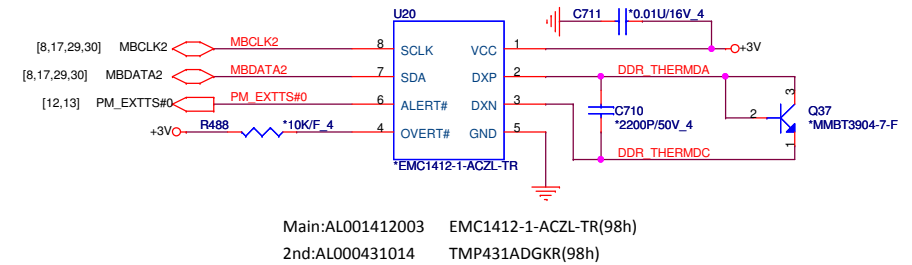




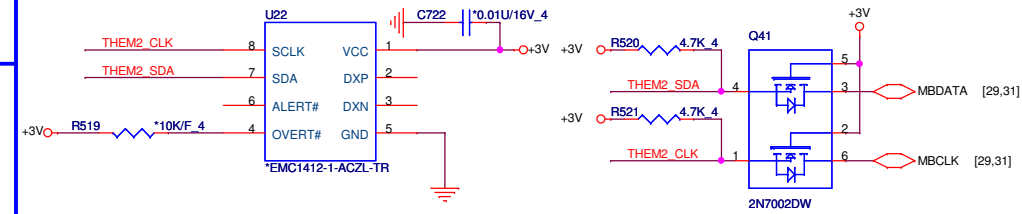
## TPM (1.2)



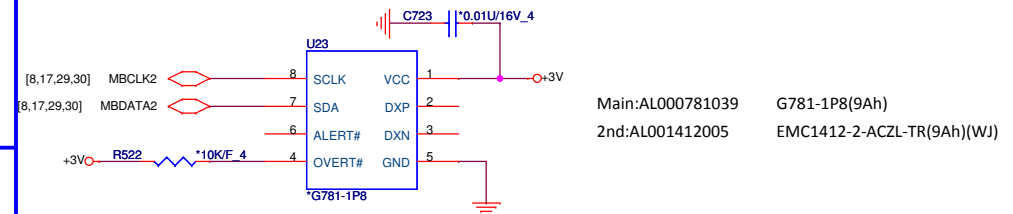
## DDR3 Thermal Sensor



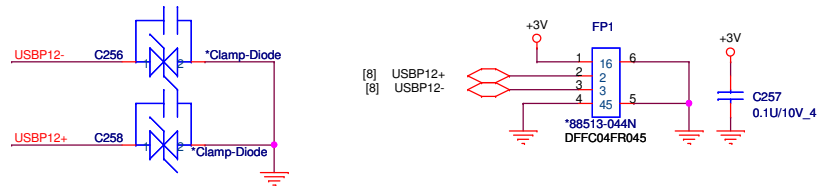
## Thermal Solution(Close to CRT)



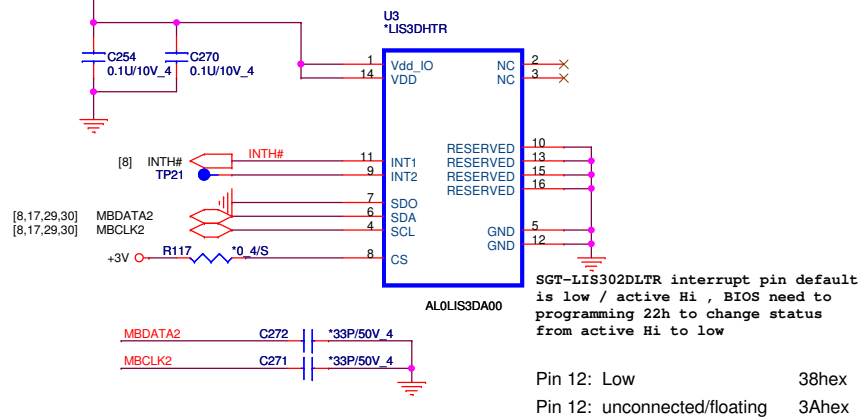
## Thermal Solution(Close to GPU)

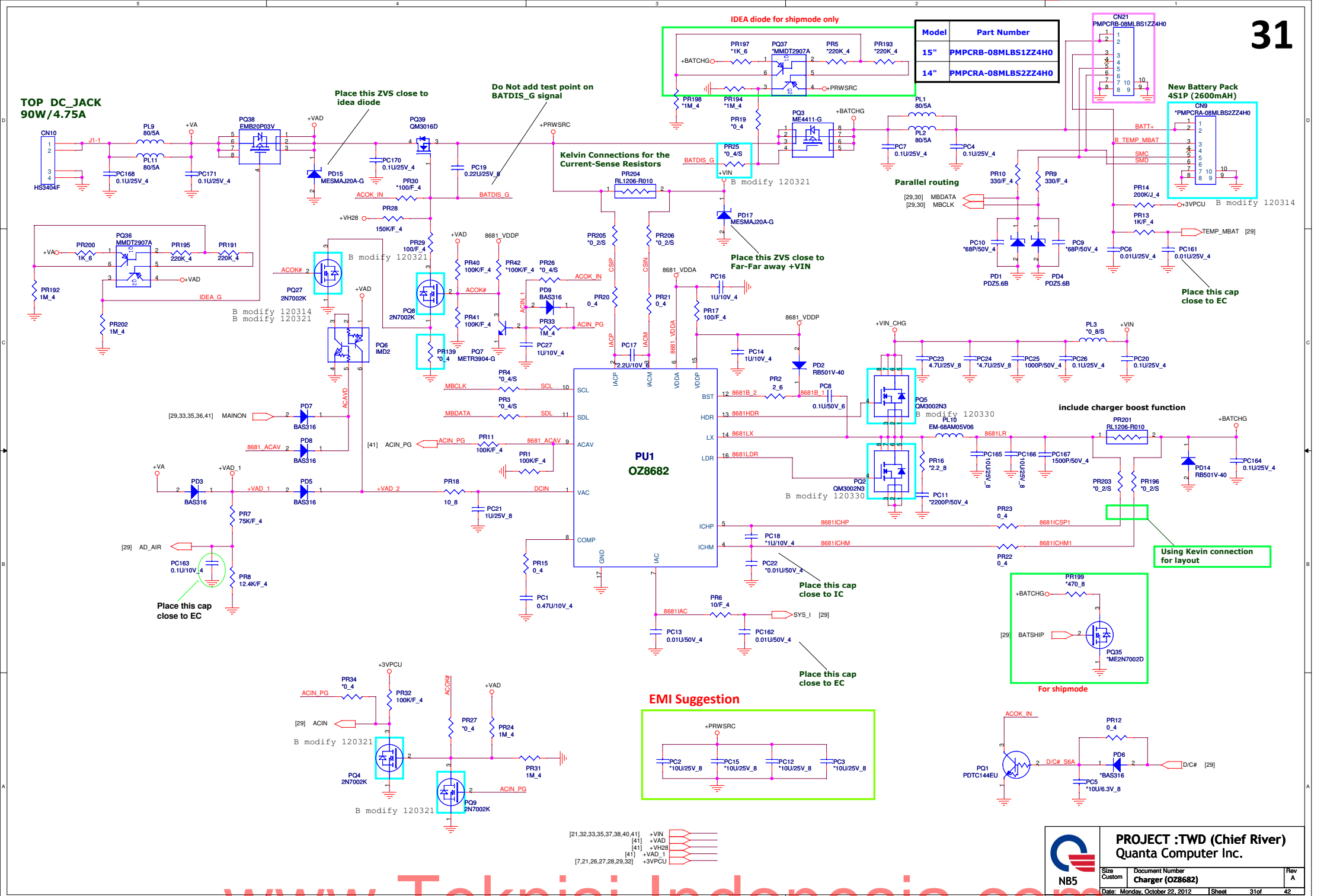


## Finger Printer



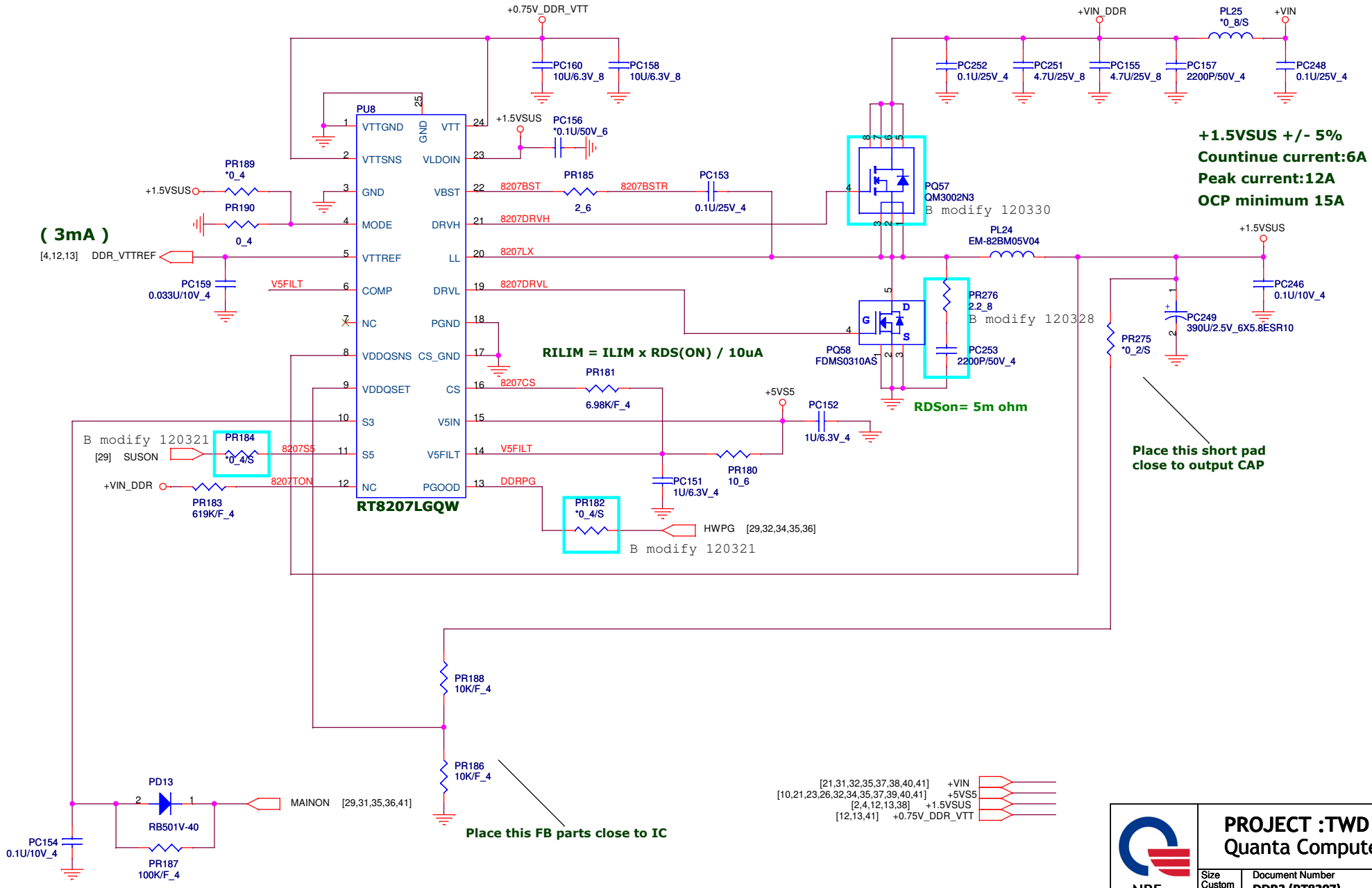
## Accelerometer Sensor(WJ)








( VTT/2A )



**+1.5VSUS +/- 5%**  
**Countinue current:6A**  
**Peak current:12A**  
**OCP minimum 15A**

**Place this short pad  
close to output CAP**

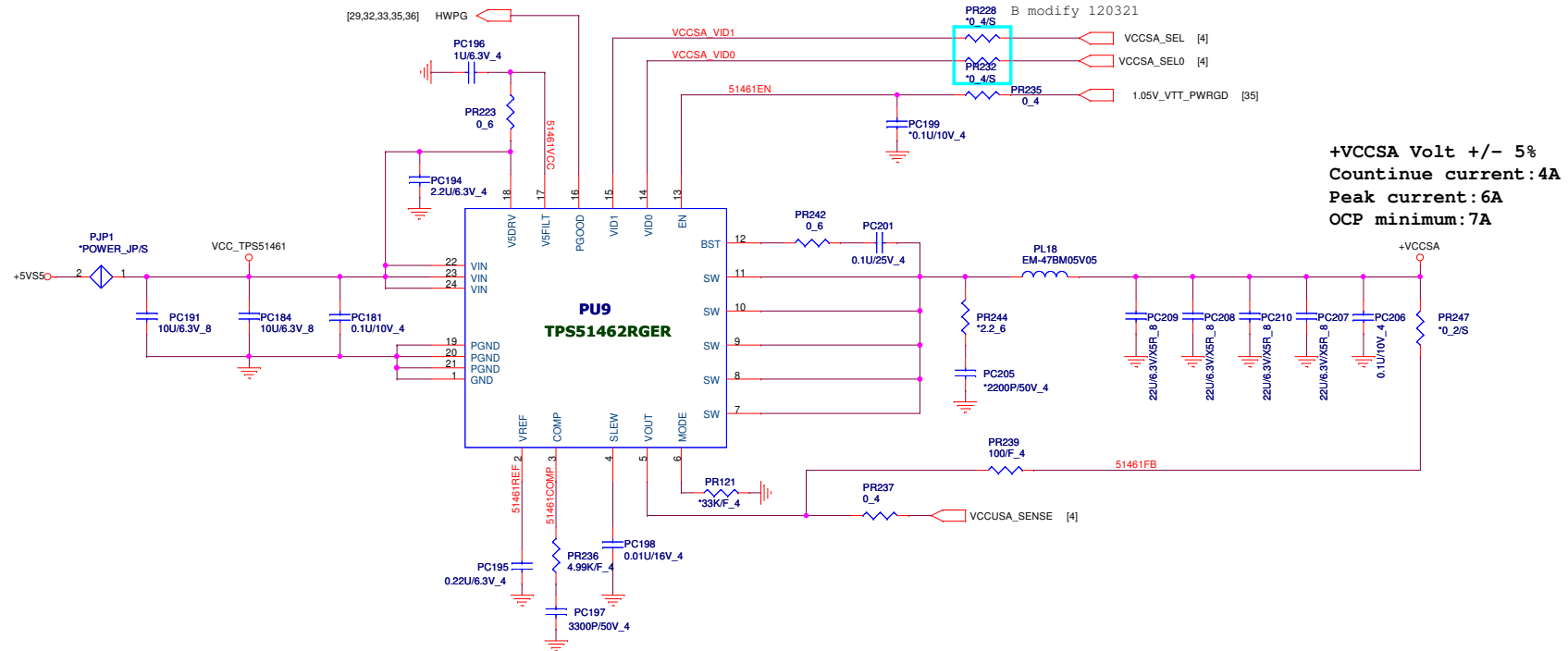
**Place this FB parts close to IC**

 NB5	<b>PROJECT :TWD (Chief River)</b> <b>Quanta Computer Inc.</b>		
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CPU system agent  
voltage slew rate of 0.5 -10 mV/ $\mu$ s

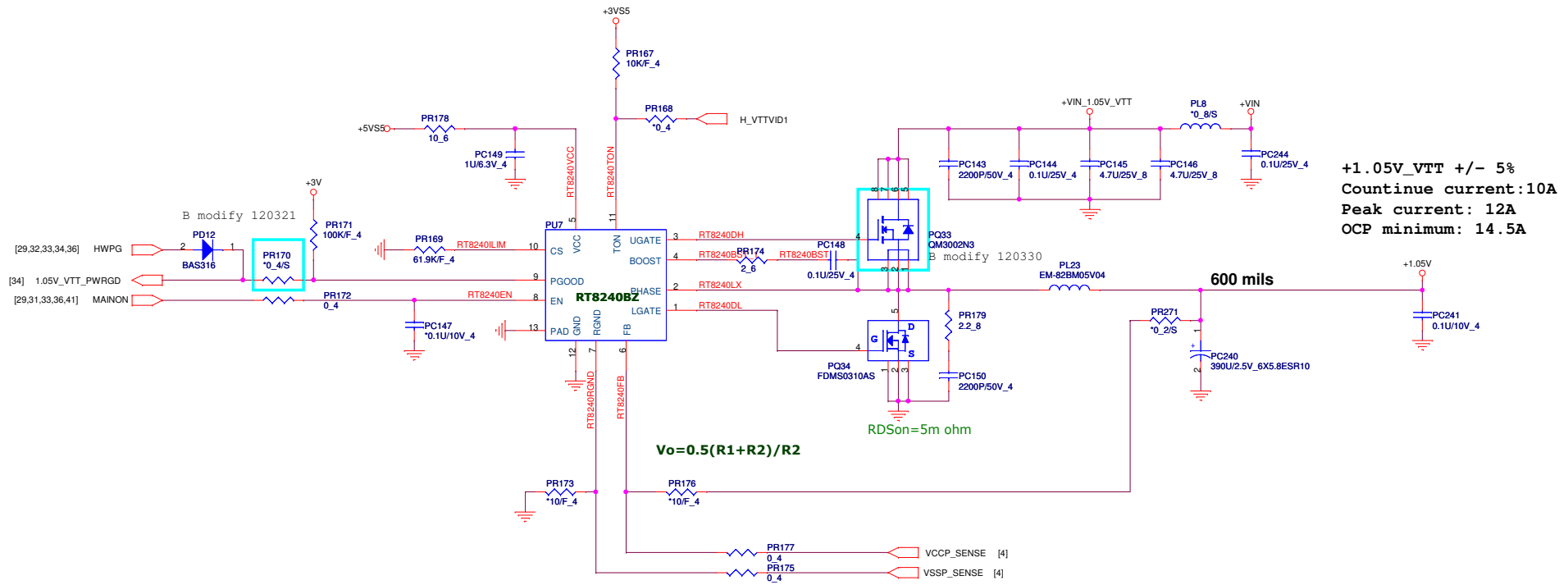
SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

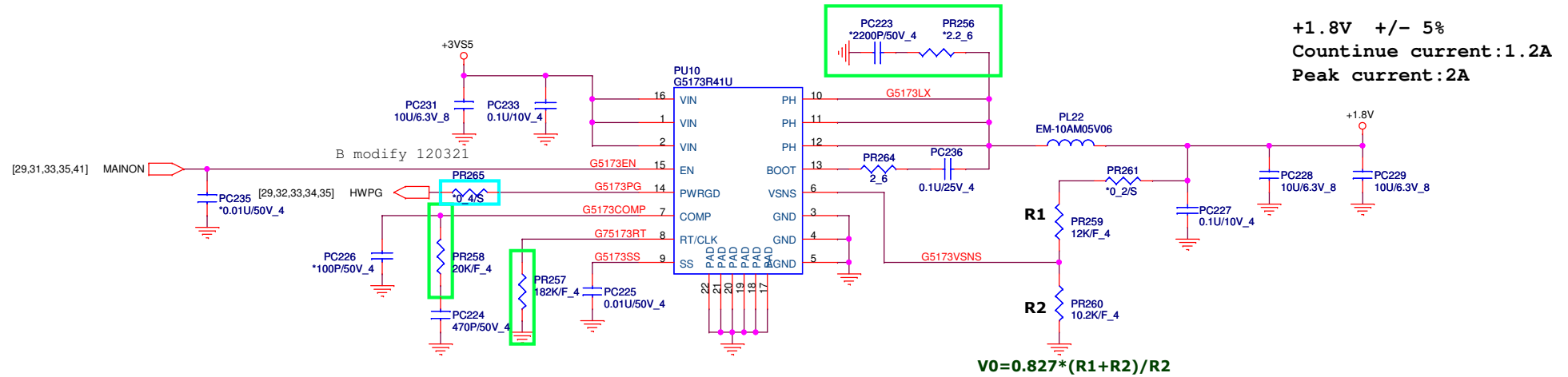
### TPS51462RGER for SV CPU



+VCCSA Volt +/- 5%  
Countinue current:4A  
Peak current:6A  
OCP minimum:7A







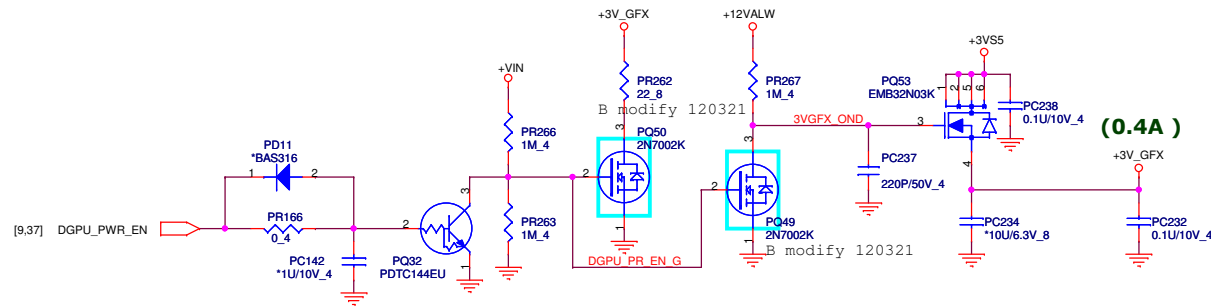
**PROJECT :TWD (Chief River)**  
**Quanta Computer Inc.**

Size B	Document Number <b>+1.8V (G9661)</b>	Rev A
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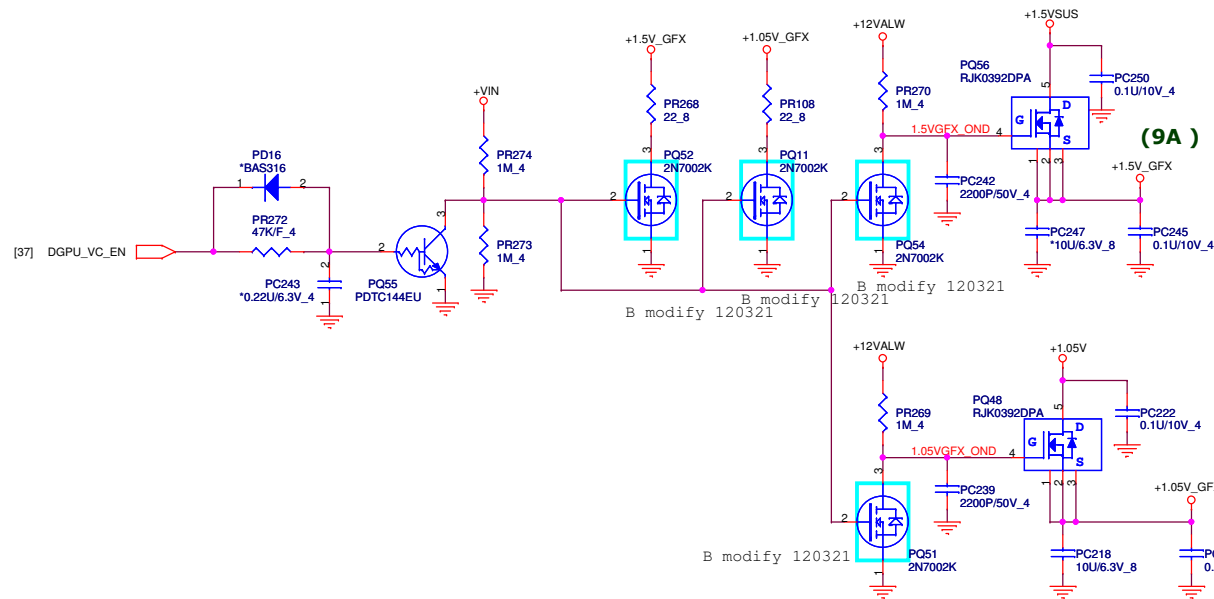
### Connect to input caps



[2,4,12,13,33]	+1.5VSUS
[10,21,26,27,29,30,32,35,36,41]	+3VSS
[14,16,17,18,37]	+3V_GFX
[15,18,19,20]	+1.5V_GFX
[14,15,16,18]	+1.05V_GFX
[41]	+12VALW
[2,4,6,7,8,10,26,29,35,39]	+1.05V

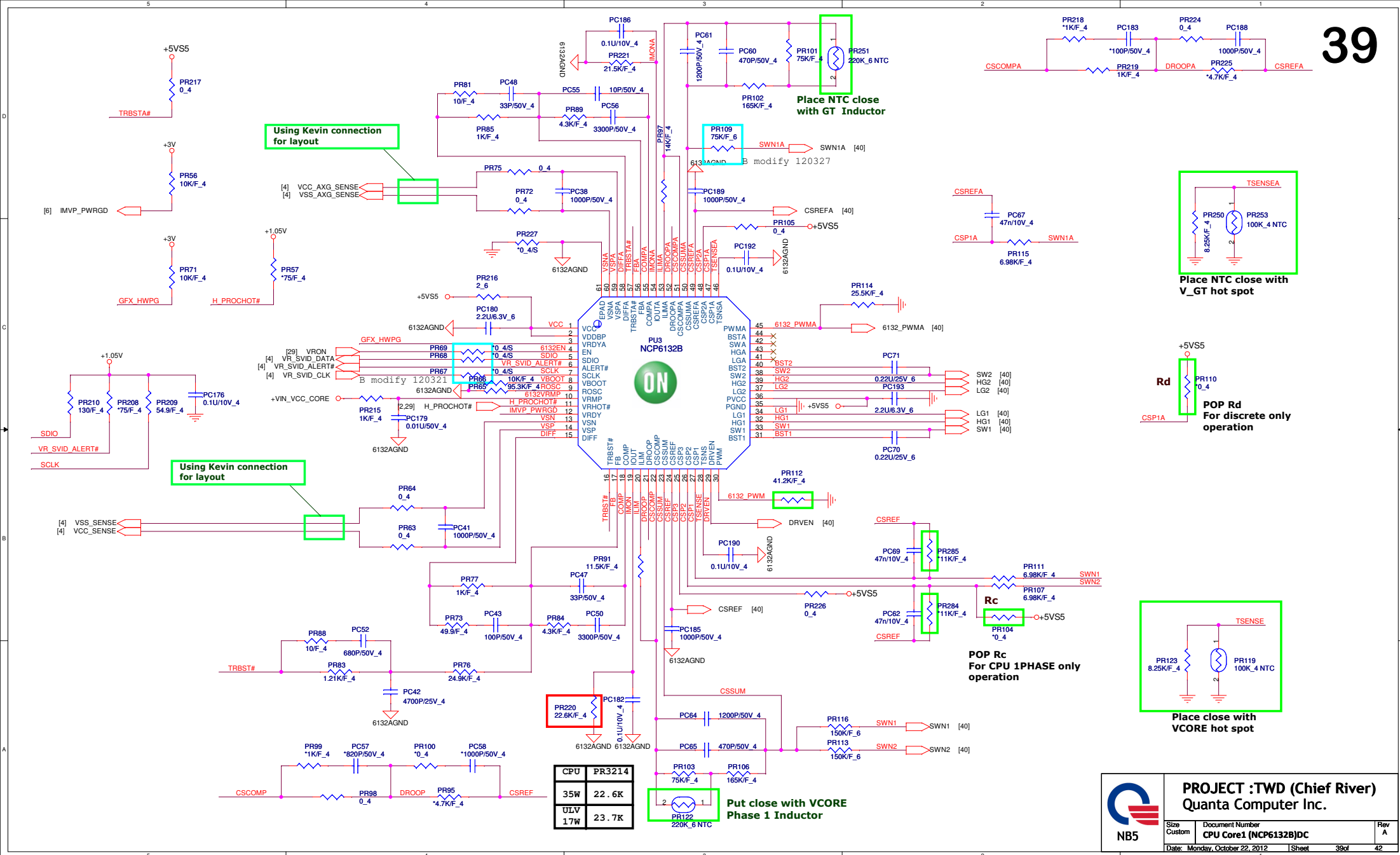


(0.4A)

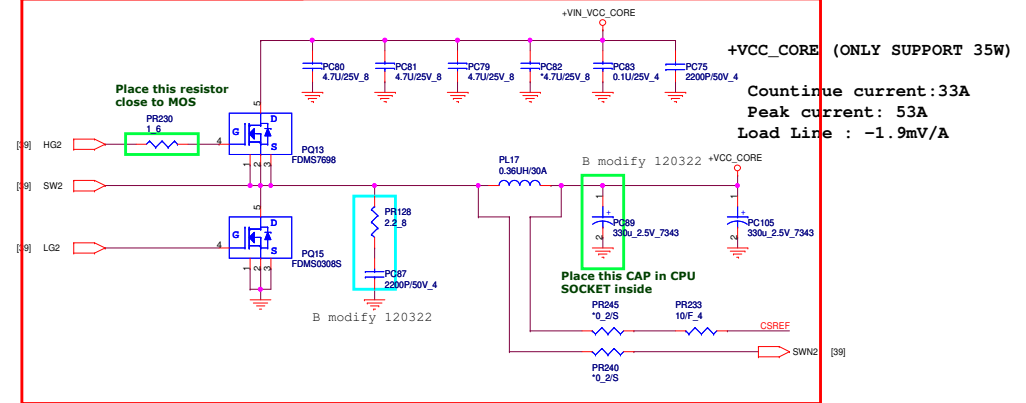
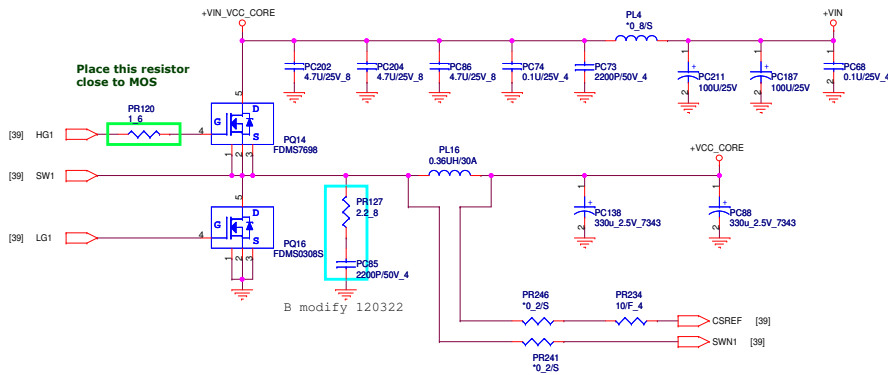


(9A)

+1.05V +/- 3%  
 Countinue current:2.1A  
 Peak current:3A



Dummy This Schematic  
For CPU 1-Phase operation

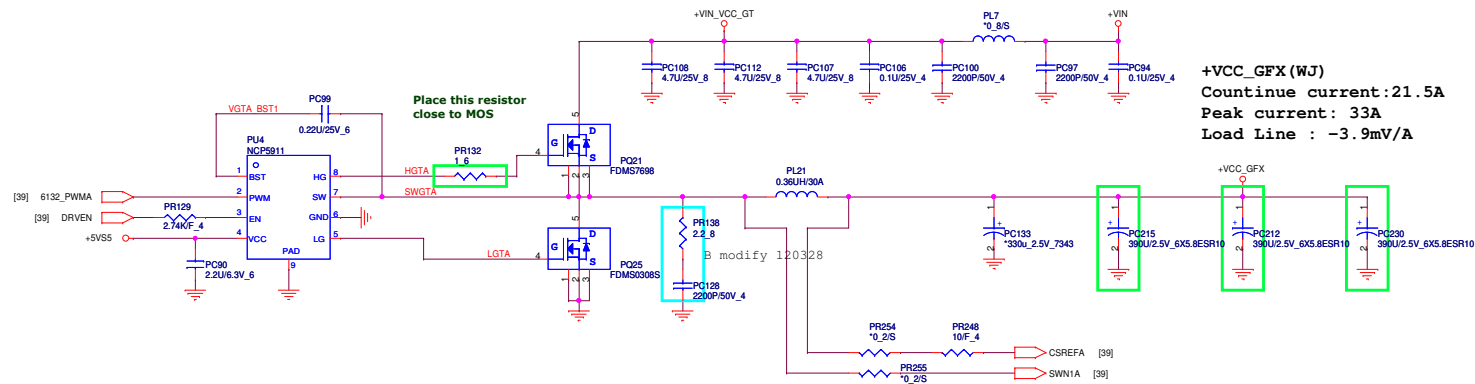


+VCC\_CORE (ONLY SUPPORT 35W)

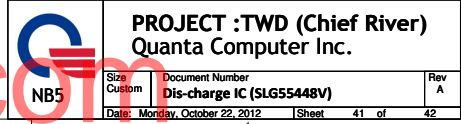
Countinue current:33A  
Peak current: 53A  
Load Line : -1.9mV/A

+VCC\_CORE (ULV 17W)

TDC : 25A  
Peak current: 33A  
Load Line : -2.9mV/A










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